Motor Driver PCB Layout Guidelines – Part 2

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The first part of this article provided some general recommendations for designing printed circuit boards (PCB) using motor driver ICs, which require careful PCB layout for proper performance. Part 2 will discuss some specific PCB layout recommendations for using typical motor driver IC packages.

Layout for Leaded Packages

Standard leaded packages, like the SOIC and SOT-23 packages, are often used for low-power motor drivers (see Figure 6).

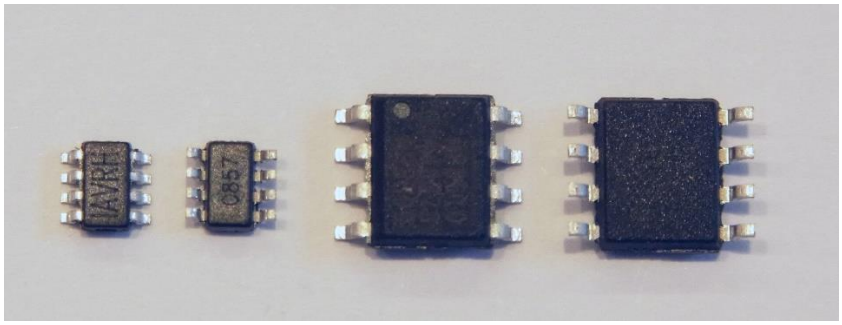

Figure 6: SOT-23 and SOIC Packages

To maximize the power dissipation capability of leaded packages, MPS uses a “flip-chip on leadframe” construction (see Figure 7). The die is bonded to the metal leads using copper bumps and solder without the use of bond wires. This allows heat to be conducted from the die through the leads to the PCB.

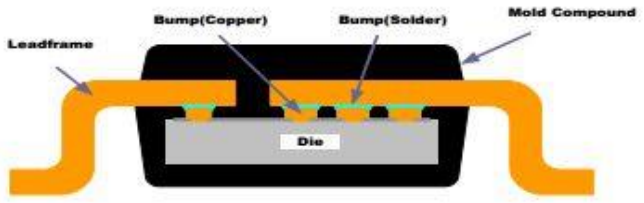

Figure 7: Flip Chip On Leadframe Structure

To maximize thermal performance, large copper areas should be attached to the leads that carry high current. On a motor driver IC, typically the power, ground, and output pins are attached to the copper areas.

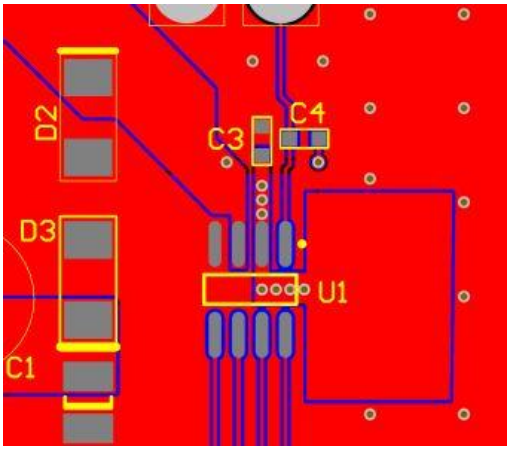

Figure 8: Flip-Chip SOIC PCB Layout

Figure 8 shows a typical PCB layout for a flip-chip on leadframe SOIC package. Pin 2 is the device power pin. Notice that a copper area is placed near the device on the top layer, and several thermal vias connect this area to copper on the backside of the PCB. Pin 4 is the ground and is connected to the copper ground pour on the top layer. Pin 3 is the device output, which is routed to a large copper area as well.

Note that there are no thermal reliefs on the SMT pads; they are connected to the copper areas solidly. This is critical for good thermal performance.

QFN and TSSOP Packages

TSSOP packages are rectangular in shape and use two rows of pins. TSSOP packages used for motor driver ICs usually have a large exposed pad on the underside of the package that is used to remove heat from the device (see Figure 9).

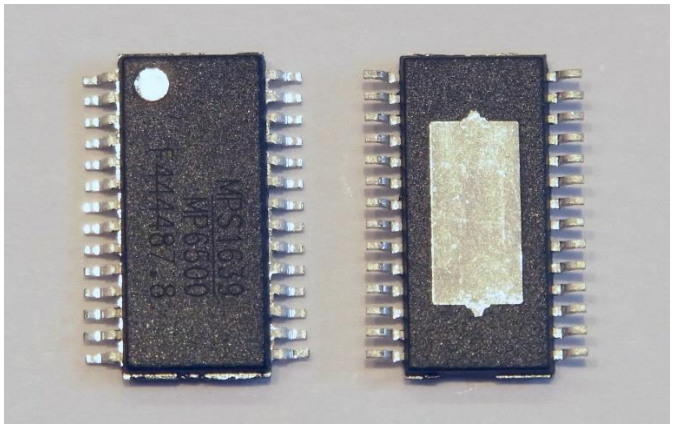

Figure 9: TSSOP Package

QFN packages are leadless packages that have pads around the outside edges of the part, as well as a larger pad centered on the underside of the device (see Figure 10). This larger pad is used to extract heat from the die.

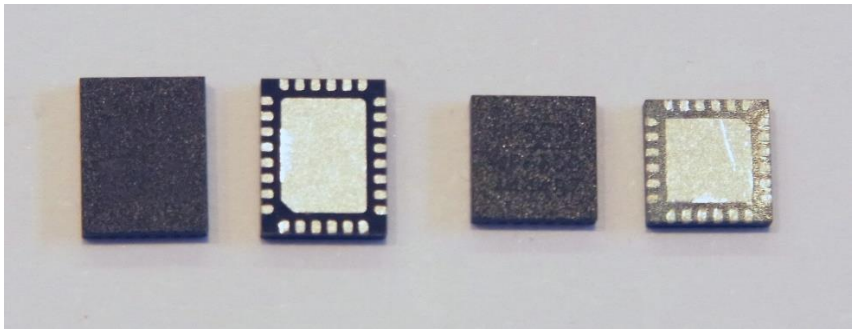

Figure 10: QFN Packages

To remove heat from these packages, a well-soldered connection must be made to the exposed pad. This pad is at ground potential normally, so it can be tied into the PCB ground plane. Ideally, thermal vias are placed in the pad area directly. In the example shown in Figure 11 below, an array of 18 vias is used with a finished hole diameter of 0.38mm. This via array has a calculated thermal resistance of about 7.7°C/W.

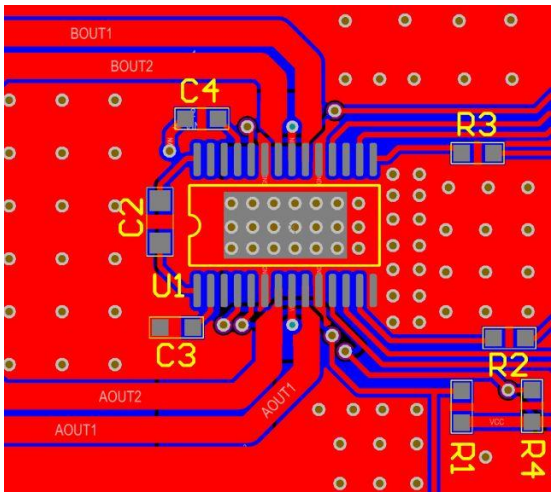

Figure 11: TSSOP PCB Layout

Normally, finished hole sizes of 0.4mm and smaller are used for these thermal vias to prevent solder wicking. If smaller holes are required by the SMT process, more holes should be used to keep the overall thermal resistance as low as possible.

In addition to the vias placed within the pad area, thermal vias are also placed in areas outside the IC body. In TSSOP packages where copper areas can extend beyond the ends of the package, this provides another path for heat to pass from the device through the top copper layer.

With QFN devices, there are pads on all four edges of the package that prevent the use of copper in the top layer to extract heat. The use of thermal vias is mandatory to pull heat out to either an inner plane or the bottom layer of the PCB.

The PCB layout below shows a small QFN (4mmx4mm) device (see Figure 12). Only nine thermal vias fit in the exposed pad area. Because of this, the thermal performance of this PCB is not as good as the TSSOP package shown in Figure 10.

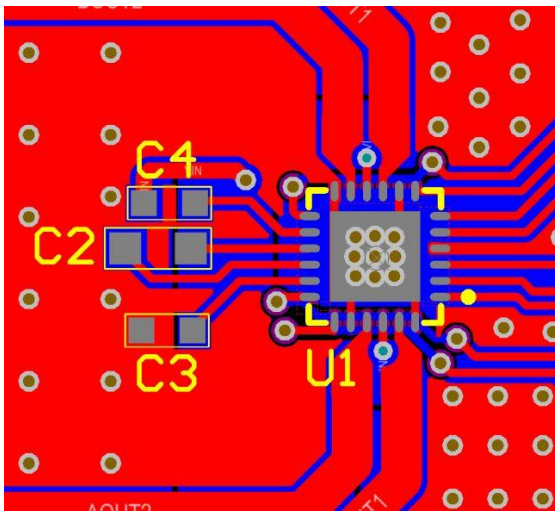

Figure 12: QFN (4mmx4mm) Layout

Flip-Chip QFN Packages

Flip-chip QFN (FCQFN) packages are similar to regular QFN packages, but instead of using wire bonds to connect the die to the package pads, the die is flipped upside-down and connected to the pads on the underside of the device directly. The pads can be placed opposite the heat-generating power devices on the die, so they are often arranged as long stripes instead of small pads (see Figure 13).

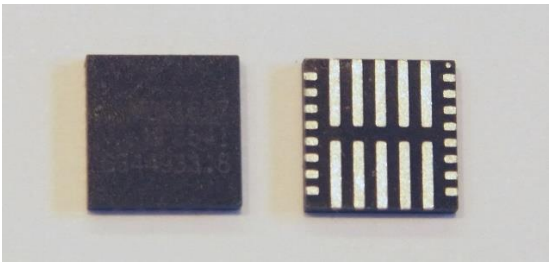

Figure 13: FCQFN Package

These packages use rows of copper bumps on the surface of the die, which are then bonded to the leadframe (see Figure 14).

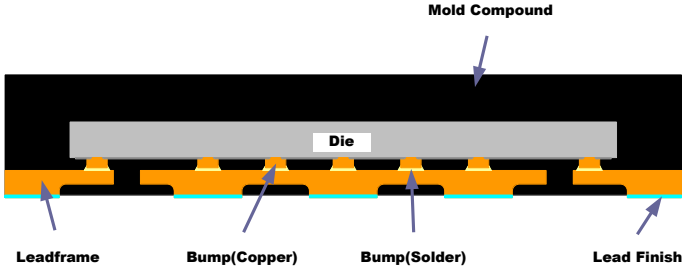

Figure 14: FCQFN Structure

FCQFN packages may have irregularly shaped pads often arranged in long, narrow stripes. Unlike normal QFN packages, heat is extracted through many of these pads instead of one large central pad. This creates a bit of a challenge for the PCB design, since there are many pads, all carrying different signals, that need copper areas connected to them.

Small vias can be placed within the pad areas, similar to what is done with regular QFN packages. On multi-layer boards with power and ground planes, vias can connect these pads to planes directly. In other cases, copper must be attached to the pads directly to draw heat away from the IC into larger copper areas.

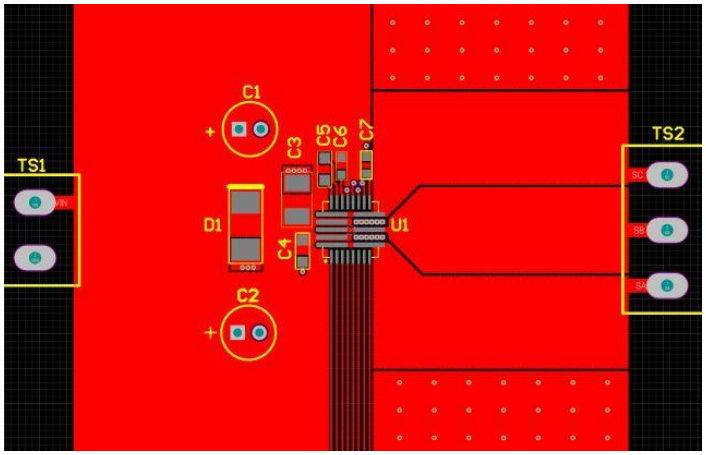

Figure 15: FCQFN PCB Layout

Figure 15 shows a PCB layout for an MP6540 power stage IC. This device has long pads for power, ground, and the three outputs. Note that the package is only 4mmx4mm.

The copper area to the left of the device is the power input. This large copper area is connected to the two power pads of the device directly.

The three output pads are connected to copper areas to the right of the device. Note how the copper area is expanded as much as possible just after exiting the pad. This provides good heat transfer from the pad to the ambient air.

Note the rows of small vias within two of the pads at the right side of the device. These pads are connected to ground, and a solid ground plane is placed on the backside of the PCB. These vias are 0.46mm in diameter with a finished drill hole of 0.25mm. The vias are small enough to fit within the pad area.

Careful PCB layout is necessary to implement successful designs using motor driver ICs. This article has presented some practical suggestions to help PCB designers achieve good electrical and thermal performance.