HR1211

Multi-Mode PFC + Current Mode LLC Controller

Application Note

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1. INTRODUCTION

The HR1211 is a combination controller that integrates Multi-Mode PFC and Current Mode HB LLC controllers and exhibits very high performance. Please refer to the HR1211 datasheet for more details.

1.1 Key Features

1. General features
    - High-voltage current source for start-up
    - Smart X-cap discharger when AC unplugged
    - UART interface for Parameters Programming
    - User-friendly GUI for optimizing PFC and LLC design
2. Power factor correction (PFC) controller
    - Patented CCM/DCM Multi mode PFC control with high efficiency from light loads to full loads
    - High PF due to Input Cap Current Compensation
    - Programmable frequency jittering for lower EMI level
    - Accurate regulation and auto-adjustable output voltage
    - Digital PI for voltage loop compensation
3. Half-bridge LLC controller
    - 600V high-side gate driver with an integrated bootstrap diode and high dV/dt immunity
    - Current Mode Control
    - Adaptive dead-time adjustment with minimum and maximum limit
    - Skip/Burst mode switching at light load
    - Programmable Soft-start
4. Protections
    - Precise brown-in/brown-out protection (programmable threshold and de-bounce timer)
    - Cycle-by-cycle current limit of the PFC
    - PFC output over-voltage protection (OVP)
    - Programmable open-loop protection(OLP) of the PFC
    - LLC Short Circuit Protection (OCP)
    - LLC Over Power Protection (OPP)
    - SO pin for external Protections
    - LLC Capacitance Mode Protection
    - Thermal Shutdown (TSD)

1.2 Block Diagram

Figure 1 shows the block diagram of the IC. The functions are described below:

1. Power supply management

   The power supply section of the HR1211 includes a high-voltage current source (HVCS) for IC start-up and two LDOs to supply the internal circuits of the IC and gate driver. The HVCS also acts as an X-cap discharger, which discharges X-cap when the AC input disconnected.

2. Digital PFC controller

   HR1211 implements a digital control scheme for PFC which includes digital control logics, ADC, DAC and comparators to achieved PFC function:

   - A 12-bit ADC, which senses the inductor current (CSP).
   - A 10-bit ADC, which senses the AC input voltage (ACIN), PFC output voltage (FBP), and LLC feedback (FBL).
   - A 10-bit DAC, which produces a signal to turn on the PFC gate in CCM.
   - Three 8-bit DACs: one DAC that produces a programmable reference for AC Brown-in/out comparator, the other one that produces a programmable reference for the OCL comparator, and the third one that produces a programmable reference for the OVP comparator.
   - PFC digital core, such as a control algorithm, digital PI loop, and calculation block.

   The digital PFC can change operation modes from CCM to DCM. At light load, the switching frequency is reduced, improving light-load efficiency.

3. Digital HB LLC controller

   HR1211 implements a digital current mode control scheme for HB LLC which is used to generate a regulated and isolated output voltage form DC bus:

   - A 10-bit DAC, which produced a reference for Reset comparator to turn off the high-side gate in soft start, skip mode and burst mode.
   - Two 8-bit DACs: one DAC that produces a programmable reference for Over-Power-Protection comparator, and another DAC that produces a programmable reference for ADOFF comparator.
   - LLC digital core, such as a control algorithm, calculation block and adaptive dead time control bock.

4. MTP and UART Communication

   HR1211 implements MTP (Multiple-Time Programmable) memory as the NVM (None-Volatile Memory). The memory organization is 128 x 16bits which can store at most 256 bytes data internal the IC. When the digital core and MTP is power-on, HR1211 automatically loads all the parameter data from MTP to RAM (Random Access Memory) for running. Users can also program customized parameter data to MTP through RAM according to different applications.

   HR1211 has a standard UART interface. With UART, it can read and write the MTP data through RAM. It can send command to load the data from MTP to RAM or load the data from RAM to MTP with the graphic user interface (GUI).

   Considering the security of the users' data, HR1211 also supports encryption to protect the data stored in NVM from reading or re-writing. By writing a nonzero 16bits password in the register (address 01h), the NVM of the IC enters read-write protection, in which condition no data can be read or write. The users can write this password into the specific register (address 7Dh) to un-lock this read-write protection status.

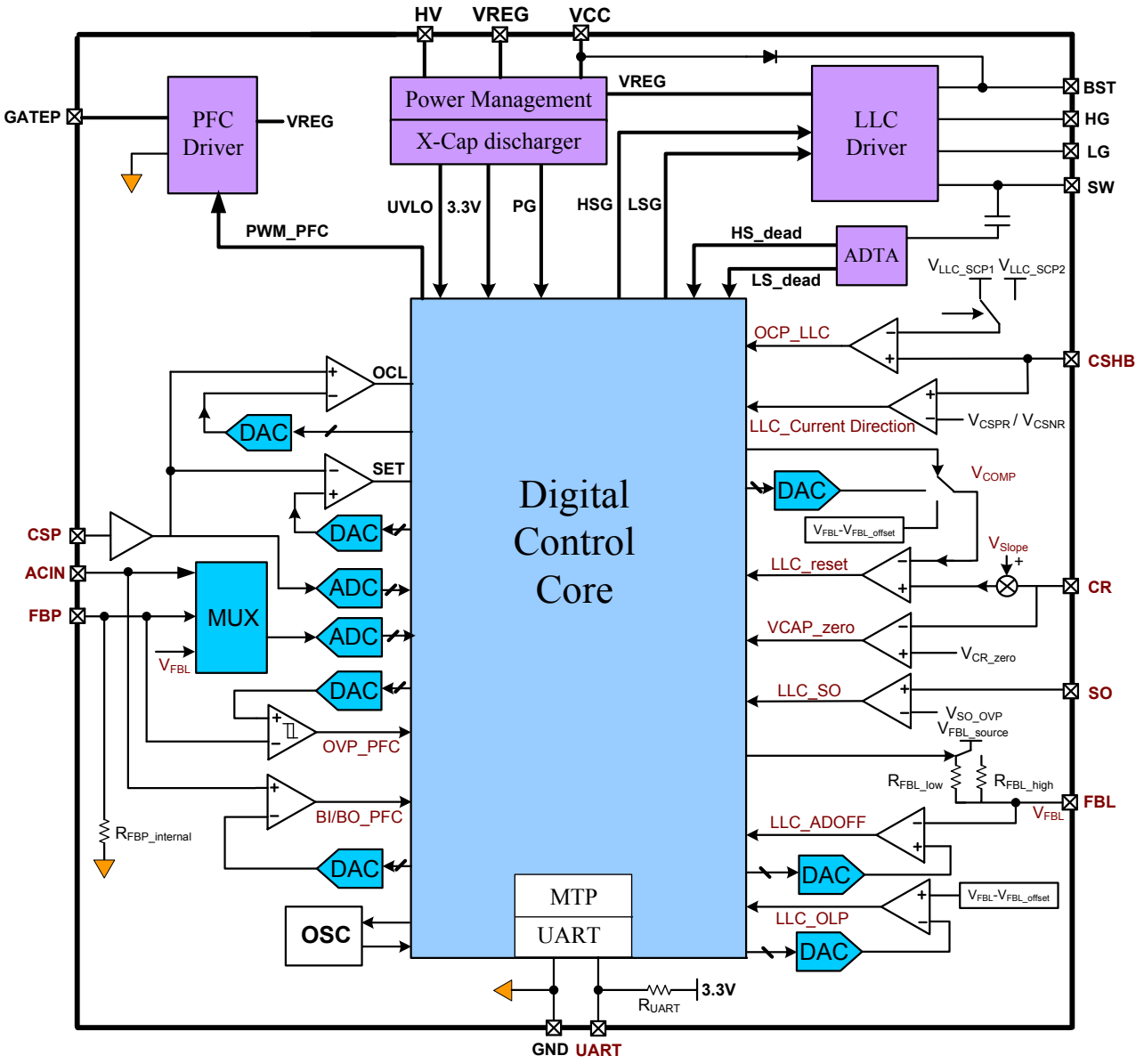


Figure 1: Block Diagram of the HR1211

1.3 Pin Descriptions

Table 1: Pin Descriptions of the HR1211

Package Pin #	Name	Description
1	FBP	Senses PFC output voltage to perform PFC switch on-time calculation, OVP & OLP protection and calculate digital current reference $I_{ref(n)}$ which decide the PFC switching frequency. A 3.3MΩ pull-down resistor is connected internally.
2	ACIN	Senses AC input voltage to perform PFC switch-on time calculation, brown in/out protection and calculate digital current reference $I_{ref(n)}$ which decide the PFC switching frequency.
3	CSP	PFC switching current sensing which defines the PFC switch on timing, switching frequency and cycle by cycle current limiting protection.
4	PGND	Ground reference of PFC and LLC Low side gate.
5	GATEP	PFC Gate Driver output.
6	VREG	Provide regulated voltage for PFC and LLC gate drivers and internal circuits.
7	LSG	LLC low-side Gate Driver output.
8	VCC	IC supply power, VCC can be charged by internal current source through HV or by external power supply.
9/14	NC	No connection.
10	HV	High voltage supply input for internal HV start-up current source and X-cap discharger when AC input disconnected.
11	BST	Voltage bootstrap, an internal bootstrap diode is connected from VCC to this pin. Externally connect a cap to SW for driving high-side MOSFET of HB LLC.
12	HSG	LLC high-side Gate Driver output.
13	SW	High-Side Switch Source. Current return for the high-side gate-drive current. Requires careful layout to avoid large spikes below ground.
15	GNDD	Ground reference for digital core of PFC
16	CSHB	Current Sense of Half-bridge. Uses a sense resistor or a capacitive divider to sense the primary current, this pin has multiple function as following: **1. Over Current Protection:** If the current continues to build up despite the frequency increase, when V_{CSHB}>V_{CS-OCP}, OCP is triggered and bring IC into programmable protection (auto-restart or latch) **2. Capacitive Mode Protection**: At the moment of LSG turns off, CSHB compares with -80mV CMP threshold, if VCSHB>-80mV, it blocks HSG gate output until slope comes out or the CMP timer is out. At the moment of HSG turns off, CSHB compares with +80mV CMP threshold, if VCSHB<+80mV, it block the LSG gate output until slope comes out or the CMP timer is out.
17	UART	UART provides a half-duplex communication IO interface.
18	FBL	LLC output voltage feedback input, internal pulled up by a 2.6V voltage source with an internal resistor. Defines LLC switching frequency according to load condition. Activating LLC skip mode, burst mode and Over Power Protection (OPP) according to voltage level on this pin.
19	CR	LLC capacitor voltage sense input. Senses divided resonant capacitor voltage to decide the LLC switching frequency.
20	SO	This pin provides external protections such as OVP or OTP. Protection will be triggered (auto-restart or latch) when SO voltage exceeds 1.5V.

2. TYPICAL APPLICATION CIRCUIT

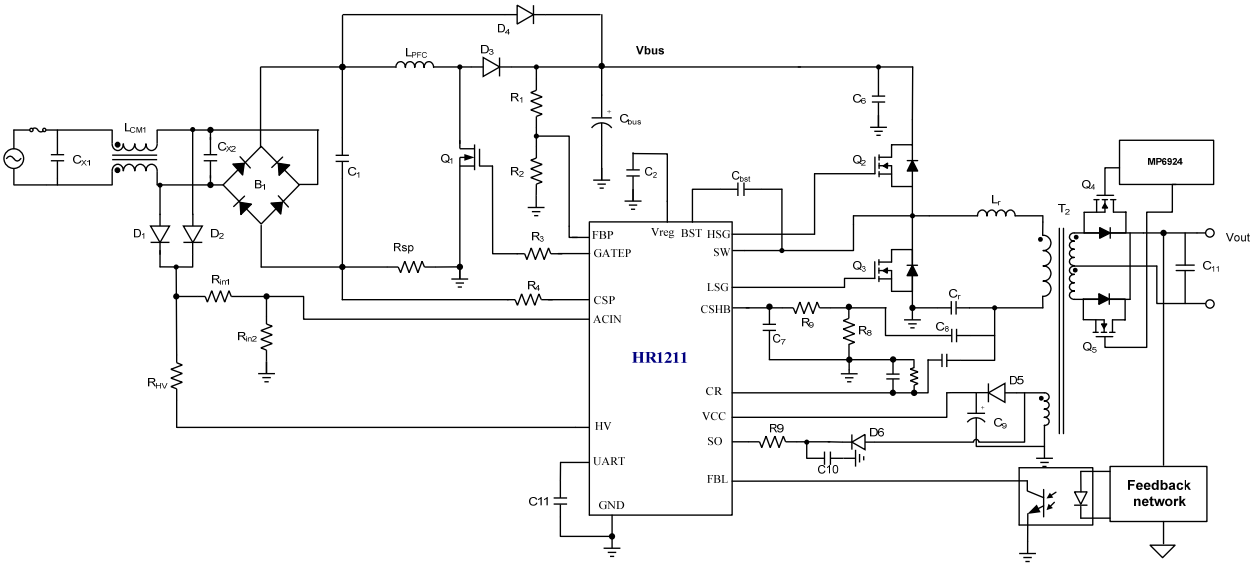


Figure 2: Typical Application Circuit

3. POWER SUPPLY FUNCTIONS

The power supply section of the HR1211 includes a high-voltage current source (HVCS) for starting up the IC, a VREG regulator for powering the gate drivers, and a 3.3V regulator for powering the digital core. The HR1211 has monitor circuits and protection circuits to make the IC more robust. Figure 3 shows an overview of the power supply circuits.

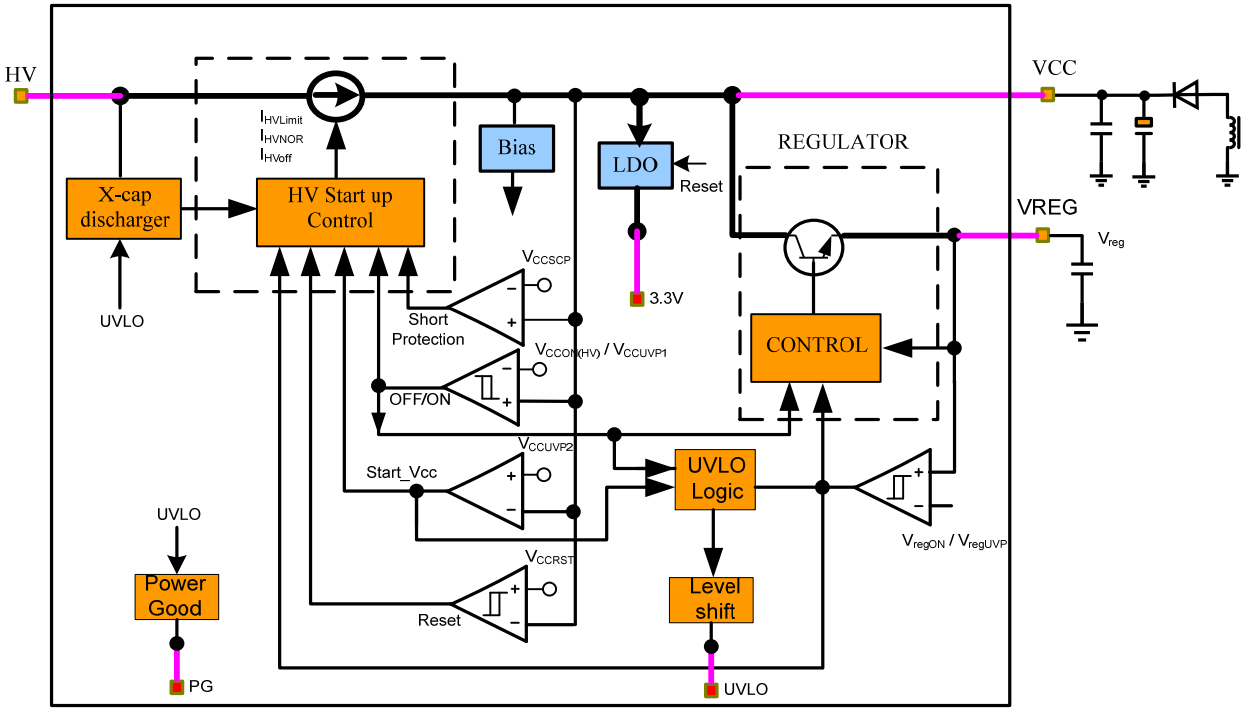


Figure 3: Overview of Power Supply

3.1 Powering the IC

3.1.1 Starting Up the IC with a High-Voltage Current Source (HVCS)

To power up the HR1211, the HV voltage should be a rectified sinusoid waveform, and the amplitude should be at least 60V. Once this condition is met, HVCS begins charging the V_{CC} cap with a current source of I_{HVNOR}. HVCS is turned off if VCC is larger than $V_{CCON(HV)}$.

Once HVCS shuts down, VCC drops down to UVP point if there is no external power supply. After that, HVCS will charge VCC up again. The operation sequence of the IC supply is shown in Figure 4.

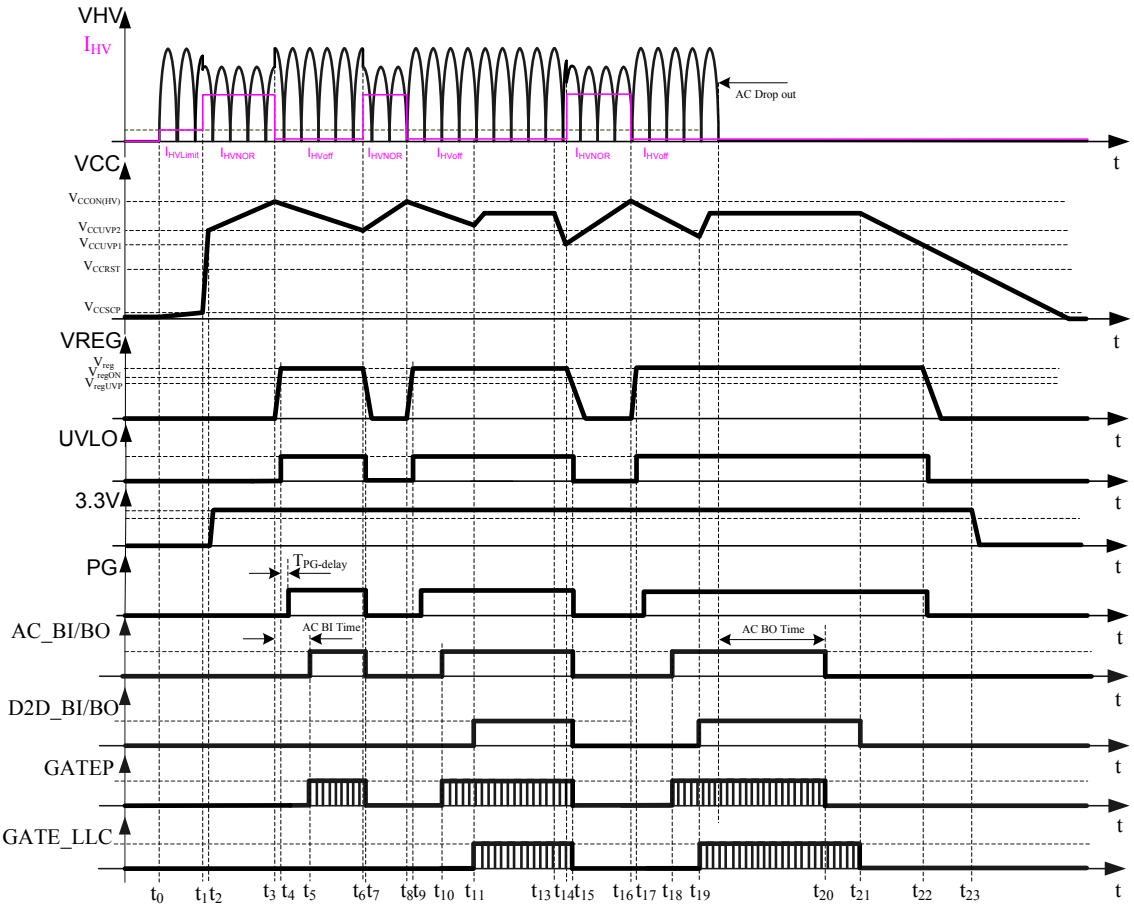


Figure 4: Operating Sequence of IC Supply

There are 2 Under Voltage Protection (UVP) thresholds of VCC. It is V_{CCUVP2} if D2D_BI/BO is low, which means LLC has not started operation yet. Otherwise, the threshold is V_{CCUVP1}. This difference is indicated at t_6 and t_{15} respectively in Figure 4.

V3.3 LDO is an internal supply for digital core, and it is enabled when VCC is higher than V_{CCUVP2} and is disabled when VCC is below V_{CCRST}.

The VREG LDO begins working when VCC reaches $V_{CCON(HV)}$ and disables at VCC UVP. The LDO of VREG is capable of providing up to 30mA of continuous current.

When VREG is higher than V_{regON} and VCC is higher than V_{CCUVP2}, both the PFC and LLC are ready to work. PFC starts switching only when AC_BI/BO is high ($V_{IN\_pk} > V_{Brown-in}$), and the LLC starts switching only when D2D_BI/BO is high ($V_{BUS} > V_{D2D\_BI}$).

3.1.2 Starting Up the IC with an External Power Supply

To power the IC from an external power supply (e.g.: standby power), the voltage applied to VCC should be larger than V_{CCUVP2} and HV should be a rectified sinusoid waveform. The IC cannot work if HV is floating or DC voltage is applied to HV.

3.1.3 Capacitor on VCC and VREG

VREG is the supply for the gate drivers of both the PFC and LLC. When the gate driver is on, larger current drawn from VREG. The capacitor on VREG should be large enough to handle this current. A ceramic capacitor of at least 10μF is recommended.

The capacitor of the external VCC must be selected carefully, as it affects both charge time (t0 to t3 in Figure 5) and discharge time (t3 to t5 in Figure 5). Generally, it requires a ceramic and electrolytic capacitor for better high-frequency noise suppression. Figure 5 shows the detail charge time and discharge time waveform.

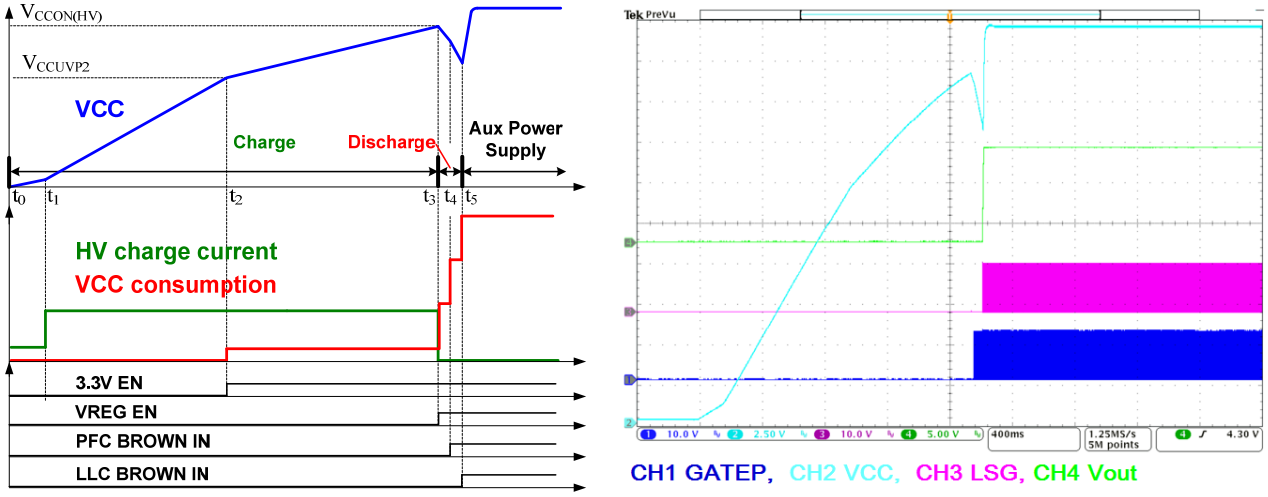


Figure 5: Start-up sequence

To select the proper capacitance, the discharge time must be long enough to sustain IC power consumption until the voltage from the auxiliary power takes over. For simplicity, the discharge time can be divided to 2 periods: AC brown in time and bulk voltage boost time. In AC brown in detection period, IC consumes I_{CC} (no switch, about 8mA). In bulk voltage boost period, IC consumes about I_{CC} (no switch) plus PFC gate driving current (gate charge times PFC operating frequency). The discharge time related with VCC capacitance and VCC voltage drop can then be calculated with Equation (1):

$$T_{discharge} = T_{AC\_BI} + T_{bulk\_boost} \approx T_{AC\_BI} + T_{PFC\_soft\_start} = C_{VCC} \cdot \frac{\Delta V1}{I_{CC\_no\_switch}} + C_{VCC} \cdot \frac{\Delta V2}{I_{CC\_no\_switch} + Q_g \cdot f_{PFC}} \quad (1)$$

$$\text{VCC Voltage Drop} = \Delta V1 + \Delta V2 < V_{CCON(HV)} - V_{CCUVP2} \quad (2)$$

Where VCC voltage drop equals ΔV1+ΔV1, and should be less than $V_{CCON(HV)}$ - V_{CCUVP2}, otherwise, the system will restart. T_{AC_BI} is the AC brown in time, $T_{PFC\_soft\_start}$ is the PFC soft start time, Q_g is the PFC MOSFET total gate charge, f_{PFC} is PFC operating frequency. According to Equation (1) and Equation (2), the minimum VCC capacitance can be calculated.

Similarly, the charge time can be divided to 3 periods: VCC SCP period (t0 to t1 in Figure 5), V3.3 disable period (t1 to t2) and V3.3 enable period (t2 to t3). In VCC SCP period, HV current source is limited with $I_{HVLimit}$ (typically 2.2mA). In V3.3 disable period, HV charge current is IHVNOR (typically 7mA). In V3.3 enable period, HV charge current keeps I_{HVNOR}, but internal digital core consumes $I_{CC\text{-}burst}$ (typically 2.2mA), so the current of charging VCC capacitor is I_{HVNOR} minus $I_{CC\text{-}burst}$. The charge time can be calculated with Equation (3):

$$T_{charge} = C_{VCC} \cdot \frac{V_{CCSCP}}{I_{HVLimit}} + C_{VCC} \cdot \frac{V_{CCUVP2} - V_{CCSCP}}{I_{HVNOR}} + C_{VCC} \cdot \frac{V_{CCON(HV)} - V_{CCUVP2}}{I_{HVNOR} - I_{CC\text{-}Burst}} \quad (3)$$

The sum of the charge and discharge time is the start-up time of the converter. If the VCC capacitor is too large, the start-up time can be too long to meet expectations.

The actual charge current is not a constant current due to HV being a sinusoid voltage. Therefore, the charge time cannot be calculated accurately. Figure 6 shows the actual charge current waveforms of HV.

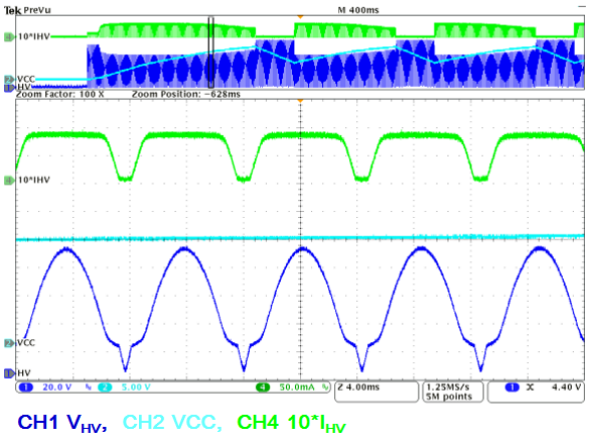


Figure 6: Current Waveform of the Charge Current

3.2 Supplying Power to VCC

3.2.1 Supplying VCC with External Voltage

The external voltage can be standby power or DC power. Generally, the VCC voltage should be above V_{CCUVP2}. To power up the IC normally when HVCS is charging VCC, a diode must be added to isolate the standby power from VCC (see Figure 7).

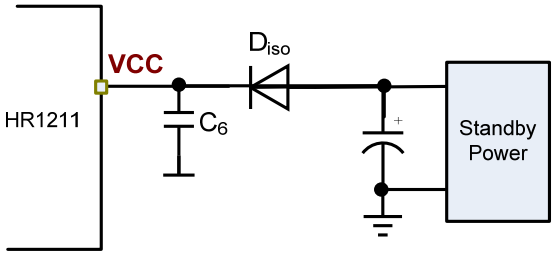


Figure 7: Supplying VCC with Standby Power

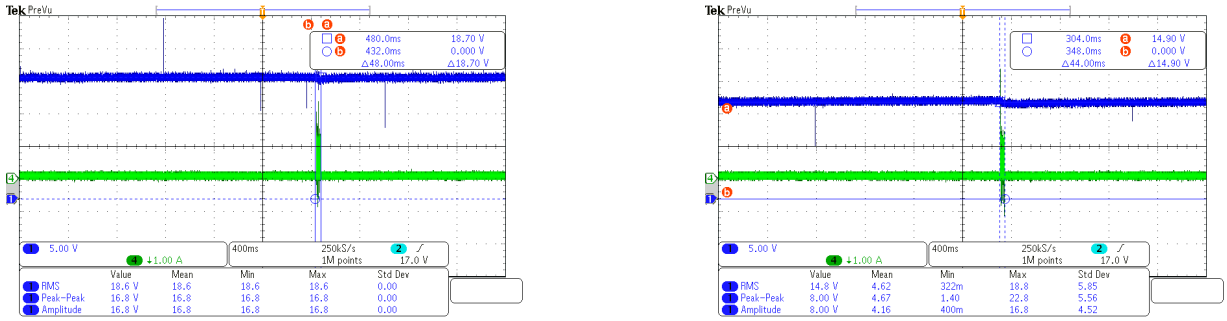
3.2.2 Supplying VCC with LLC Auxiliary Winding

For non-standby applications, VCC is supplied by the LLC auxiliary winding for higher efficiency. Figure 8 shows two types of auxiliary winding configurations: a half-wave rectifier and a full-wave rectifier. Generally, a full-wave rectifier has higher efficiency and produces a larger VCC if the turns of two windings are same, thereby increasing efficiency at light load. However, the full-wave rectifier requires another winding and rectifying diode, which increases cost.

(a) Half-Wave Rectifier **(b) Full-Wave Rectifier**

Figure 8: Supplying VCC with LLC Auxiliary Winding

R_{AUX1} and R_{AUX2} are implemented to limit inrush current. While the LLC works in burst mode at no-load condition, the resistors and capacitor C6 work as a filter, so the value of the resistors affect VCC at no load. As shown in Figure 9, the voltage of VCC is about 18.7V with 0Ω, but 14.9V with 1Ω at no-load.



a. R_{AUX1}= R_{AUX2}=0Ω **b. R_{AUX1}= R_{AUX2}=1Ω**

Figure 9: R_{AUX1} and R_{AUX2} Regulating VCC at No Load

It is recommended that the auxiliary winding be placed beside the secondary-side winding of the LLC to reduce the spike of the auxiliary winding and the VCC variation caused by output load change. N2 is the auxiliary winding of VCC placed in the slot with the secondary-side winding (see Figure 10).

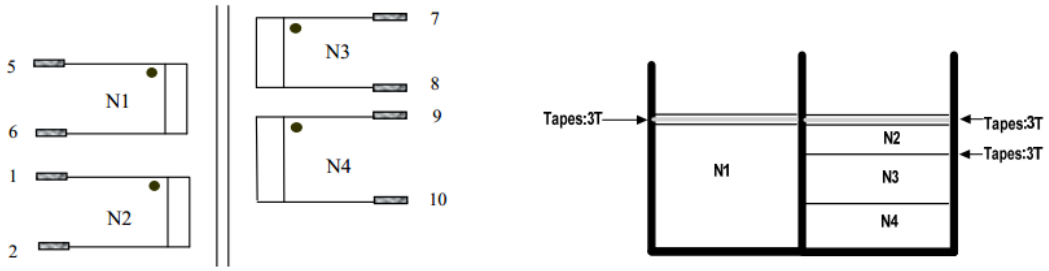


Figure 10: Auxiliary Winding Coupled Closely to Secondary Side Winding

3.2.3 VCC Current

The current consumed by VCC includes the V3.3 current, VREG current, and bias current of the internal circuit. The total current is the sum of these three currents.

In the duration of t_0 to t_2 shown in Figure 4, before V3.3 enabled, the current of VCC is about 200us. In the duration of the V3.3 enabled and before IC enable (t_2 to t_3 and t_7 to t_9), the current of VCC is $I_{CC\text{-}start1}$. Once the IC is enabled, the current of VCC is $I_{CC(nor)}$ in normal operation and $I_{CC\text{-}Burst}$ at burst-off mode.

3.3 Protection

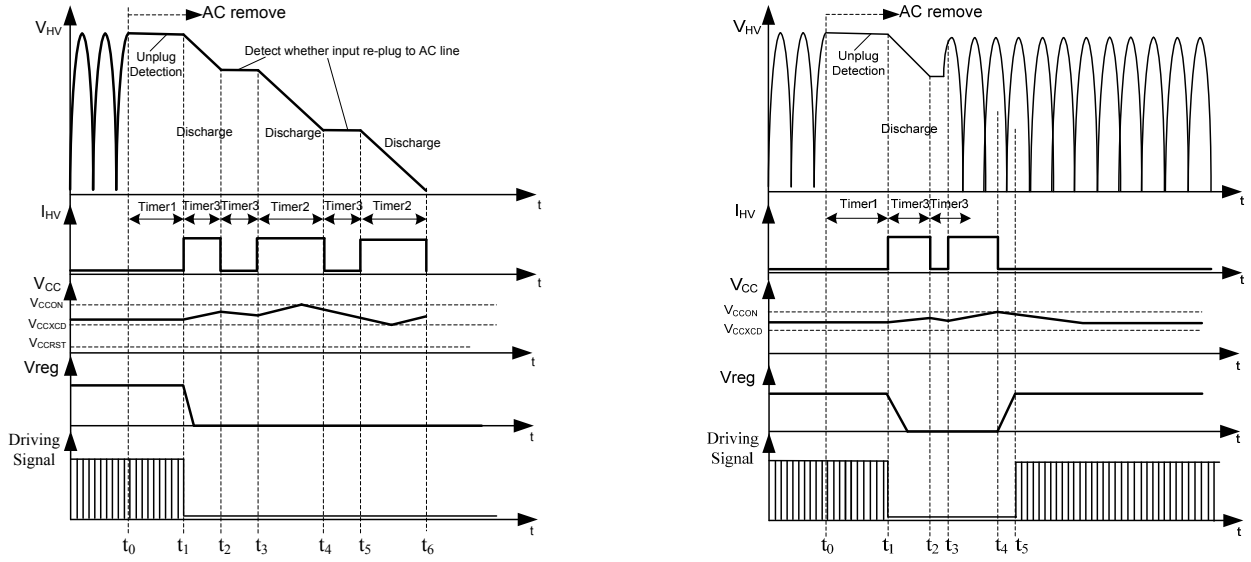
To reduce thermal stress of the IC, the HR1211 implements short circuit protection of VCC and VREG. The charge current of HV is limited to about $I_{HVLimit}$ when VCC is below V_{CCSCP}. For VREG LDO, the supply current capacity is limited to about 15mA when VREG shorts to ground.

3.4 X-Cap Discharge

For safety consideration, the voltage of the X-caps should be discharged to a safe level within a certain time when the input voltage is removed. The HVCS of the HR1211 also acts as an X-cap discharger. It monitors the AC input voltage and discharges the X-caps when the AC input is removed. Therefore, there is no need for additional resistors to discharge the X-caps, saving both component count and power.

As shown in Figure 11, the X-cap discharge function is activated when the HR1211 detects that HV voltage is DC for a detection time window Timer1 (60 x $T_{X\text{-}d}$). Firstly, HVCS discharges the X-cap

voltage and charges VCC for Time3 (30 x T_{X-d}). Then, HVCS is turned off for Timer3 (30 x T_{X-d}) and detect whether the AC input is recovered. During the detcection period, the IC recovers to normal operation if it detects that HV is no longer a DC voltage (Figure 11-b). Otherwise, the IC continues discharging during the next Timer2 (90 x T_{X-d}), then stops for Timer3 (30 x T_{X-d}) detection time, and repeats this process until the voltage of the X-cap is discharged very low (Figure 11-a).



a). AC totally removed **b). AC recovery**

Figure 11: Waveform of X-cap discharger

3.5 Surge Immunity Design Tips of VCC and HV

Surge immunity is an essential test item of any commercial power supply. Surge leads in high voltage and large inrush current to the power supply and maybe disturb the system operation, which sometimes affects performance. Noise is difficult to deal with since the coupling path is difficult to identify. For the HR1211, some design tips are provided below to help improve the surge performance.

3.5.1 HV Resistor

As shown in Figure 2, the resistor R_{HV} can help reduce voltage spikes on HV during a surge test. R_{HV} is meant to protect the IC and is recommended to be 5kΩ.

3.5.2 VCC Supply Loop

For CM surge, a stray capacitor between the primary-side winding and secondary-side winding of the LLC transformer is one key coupling path to prevent surge noise from coupling to the reference GND. There are two methods that proven effective at this (see Figure 12). In the first method, the reference ground of the auxiliary winding should be separated from the IC reference ground and connected to the power reference ground. The second method is to add a serial resistor (R_{surge}) between VCC and the electrolytic capacitor.

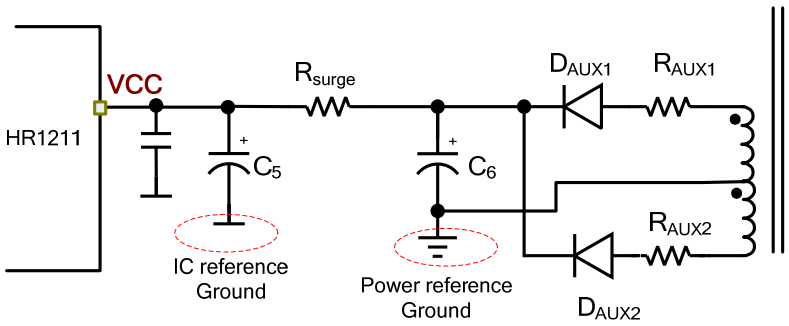


Figure 12: Separate Ground Reference of VCC

4. DIGITAL PFC FUNCTIONS

4.1 Operation of the Digital PFC

4.1.1 Sensing the Input Voltage, Output Voltage, and Inductor Current

The input voltage, output voltage, and inductor current are monitored by peripheral components of the IC (see Figure 13). The typical sensing circuitries of the digital PFC are described below.

- **ACIN** connect to a resistor divider to sense the rectified AC input voltage. The ratio of resistor divider should be fixed at 0.0032. A capacitor (C_2) is recommended to parallel with pull-down divided resistor to filter high frequency noise. The time constant of the RC filter is usually less than 100μs, otherwise, the power factor will be worse.
- **FBP** also connect to a resistor divider to sense the bulk voltage. The internal pull down resistor of 3.3MΩ should be considered when design the external resistors. Make the total divided ratio to 0.0032 according to Equation (4):

$$\frac{R_{out2} // 3.3M\Omega}{R_{out1} + (R_{out2} // 3.3M\Omega)} = 0.0032 \quad (4)$$

  A capacitor (C_3) is also recommended to parallel with R_{out2}, and the time constant of RC filter is usually between 15μs and 150μs.

- **CSP** is used to sense the inductor current
  - ➢ **R_{CS}** senses the inductor current directly. Since R_{CS} senses the PFC inductor current, the voltage on CSP is negative, so the voltage V_{CS} sensed by the 12-bit ADC is V_{CSP_BIAS} minus V_{Rcs}. Since V_{Rcs} changes with the load, R_{CS} should be designed carefully to ensure that V_{CS} is below 1.6V.
  - ➢ **R_{CSP}** connects to CSP to obstruct voltage spike in high inrush or surge test. It is recommended to be 500Ω.

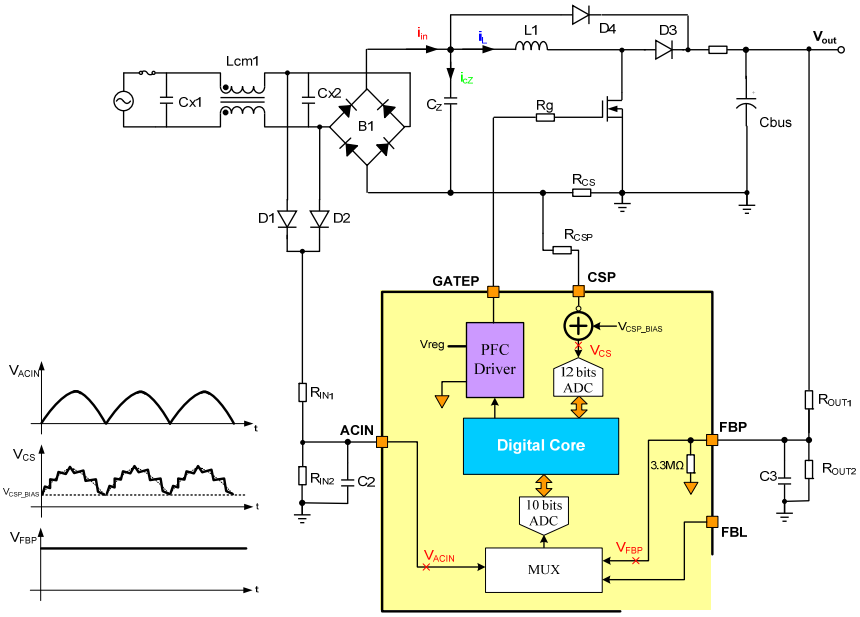


Figure 13: Typical Application Circuit of PFC

4.1.2 Operation Flow Chart in a Switching Cycle

Figure 14 shows the operation flow chart of the PFC in a switching cycle.

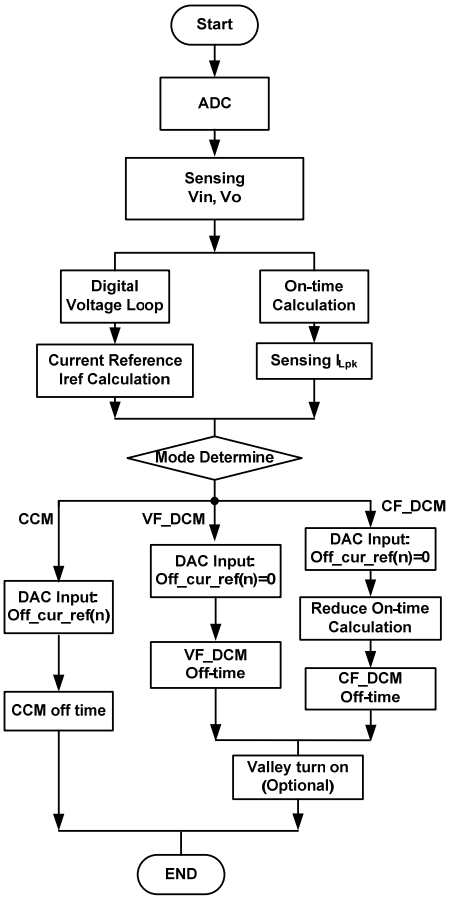


Figure 14: Flow Chart of the PFC in a Switching Cycle

4.1.3 Designing the PFC Inductor

The PFC can operate in CCM at heavy loads and low-line voltages and changes to DCM automatically at lighter loads or higher line voltages (see Figure 15). E.g. with 50Hz power grid frequency, the converter works in CCM at 85V_{rms} in full load. At 230V, the converter works partially in CCM and partially in DCM.

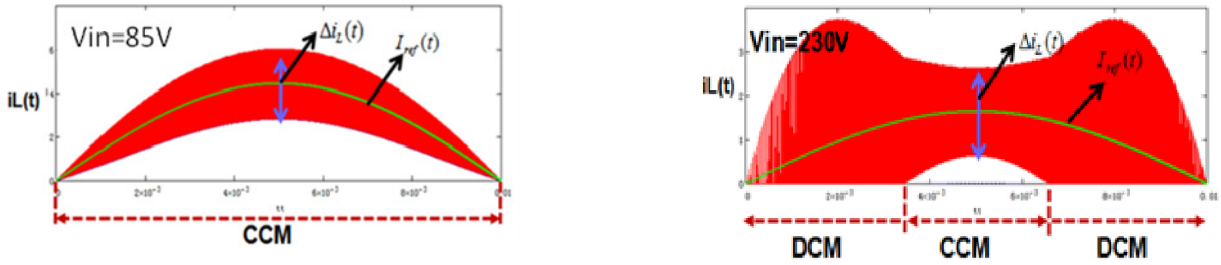


Figure 15: Waveform of the PFC Inductor in a Line Cycle

The input voltage $V_{in}(t)$ can be calculated with Equation (5):

$$V_{in}(t) = \sqrt{2} \cdot V_{in} \cdot \left|\sin(2 \cdot \pi \cdot f_{line} \cdot t)\right| \quad (5)$$

$I_{ref}(t)$ is the average current of PFC inductor and can be calculated with Equation (6):

$$I_{ref}(V_{in}, t) = \left| \frac{\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{in}} \cdot \sin(2 \cdot \pi \cdot f_{line} \cdot t) \right| \quad (6)$$

The turn-on time of the PFC MOSFET can be calculated with Equation (7):

$$T_{ON}(V_{in}, t) = \frac{(V_o - V_{in}(t))}{V_O} \cdot \frac{1}{f_{\max}} \quad (7)$$

K is the ratio of the ripple current to the average current and can be calculated with Equation (8):

$$K = \frac{\Delta i_L(V_{in\min}, \frac{1}{4 f_{line}})}{I_{ref}(V_{in\min}, \frac{1}{4 f_{line}})} \quad (8)$$

K indicates the operation mode of the PFC inductor. When K = 2, the PFC works in CrM. Knowing the value of K, the PFC inductor can then be calculated with Equation (9):

$$L = \frac{V_{in\min}(t)}{K \cdot I_{ref}(V_{in\min}, t)} \cdot \frac{(V_o - V_{in\min}(t))}{V_O} \cdot \frac{1}{f_{\max}} \quad (9)$$

The current ripple of the PFC inductor can be calculated with Equation (10):

$$\Delta i_L(V_{in}, t) = \frac{\sqrt{2} \cdot V_{in} \cdot \left|\sin(2 \cdot \pi \cdot f_{line} \cdot t)\right|}{L} \cdot T_{ON}(V_{in}, t) \quad (10)$$

In CCM operation mode, the peak current of the inductor appears at $V_{in\text{-}min}$ and full load and can be calculated with Equation (11):

$$I_{Lpk} = I_{ref}(V_{in-\min}, \frac{1}{4f_{line}}) + \frac{\Delta i_L(V_{in-\min}, \frac{1}{4f_{line}})}{2} \quad (11)$$

Once the PFC inductance (L) and maximum switching frequency are determined, the operation mode of the PFC is only determined by Po and $V_{in}(t)$. The switching frequency also changes according to different input voltages and output load conditions.

Below are the entry levels for different operation modes.

- Mode 1: CCM occurs when $I_{pk}(n) < 2I_{ref}(n)$. The switching frequency is fixed and is equal to f_{max}.
- Mode 2: VF-DCM occurs when $2I_{ref}(n) < I_{pk}(n) < 2I_{ref}(n) \cdot \frac{f_{\max}}{f_{\min}}$, the switching frequency is equal to $\frac{2 \cdot P_O \cdot L \cdot f_{\max}}{V_{in}^{\ 2} \cdot \eta \cdot Ton(V_{in}, t)}$.
- Mode 3: CF-DCM occurs when $I_{pk}(n) > 2I_{ref}(n) \cdot \frac{f_{\max}}{f_{\min}}$. The switching frequency is fixed and equal to f_{min}.

Figure 16 shows the switching frequency profile in a line cycle. At heavy load, the switching frequency is at f_{max}. When the load is reduced, the switching frequency changes to f_{min} at very light load.

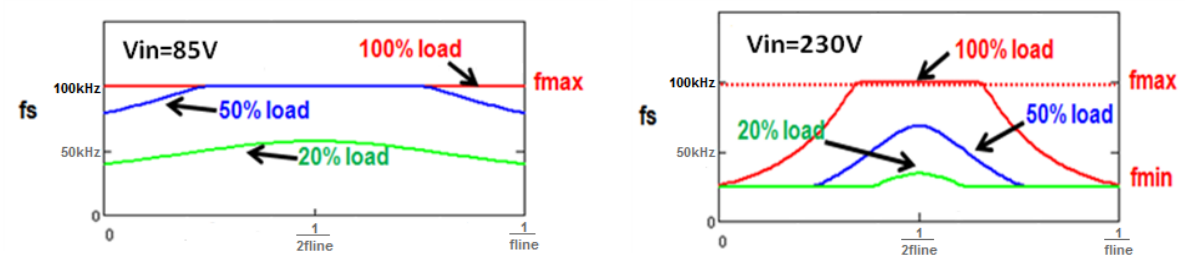


Figure 16: Switching Frequency Profile in a Line Cycle

The maximum and minimum switching frequency can be configured through the GUI of the HR1211 (see Figure 17).

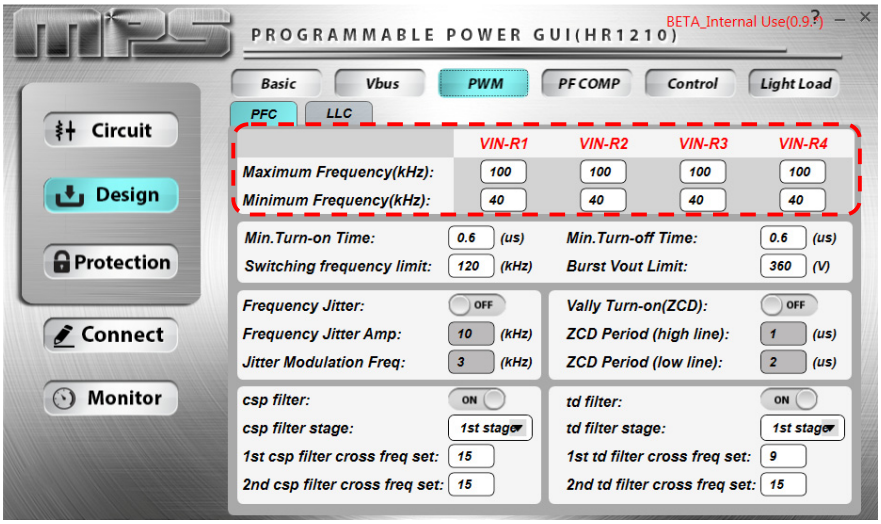


Figure 17: GUI Interface to Program Switching Frequency

The HR1211 can reduce switching frequency at light load, so the efficiency at light load is enhanced due to lower core loss and switching loss. The HR1211 has higher efficiency at light load than a conventional CrM controller (see Figure 18).

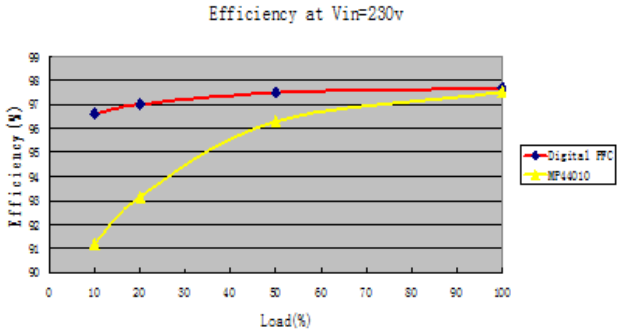


Figure 18: Efficiency Comparison between HR1211 PFC and Traditional CrM Controller

The CCM peak current of the inductor appears at V_{in-min} and full load and can be calculated with Equation (12):

$$I_{Lpk} = I_{ref}(V_{in-\min}, \frac{1}{4f_{line}}) + \frac{\Delta i_L(V_{in-\min}, \frac{1}{4f_{line}})}{2} \quad (12)$$

The CCM inductor current can then be calculated with Equation (13):

$$I_{L-rms} \approx \frac{P_{OUT}}{\eta \cdot V_{in-\min}} \quad (13)$$

The core size of the PFC inductor can be selected by calculating the AP value with Equation (14):

$$AP = \frac{L \cdot I_{Lpk} \cdot I_{L-rms}}{B_{\max} \cdot J_c \cdot K_u} \quad (14)$$

Where I_{Lpk} is the peak current (A) of the inductor (which should be calculated at the minimum input voltage and full load), I_{L-rms} is the effective current of the inductor, J_C (A/m^2) is the current density of the

winding, B_{max} (T) the maximum magnetic flux density that is allowed, and K_U is the usage ratio of winding in bobbin window (typically 0.3~0.4).

The number of turns of the PFC inductor can be calculated with Equation (15):

$$N = \frac{L \cdot I_{Lpk\_OL}}{A_e \cdot B_{max}} \quad (15)$$

Where I_{Lpk_OL} is the peak current of overload (for simplicity, $I_{Lpk\_OL} = Ratio_{OL} \cdot I_{Lpk}$). A_e is the core sectional area, B_{max} is usually taken the value of 0.28 (T). This calculated turns (N) ensures that inductance will not be saturated under overload condition. The overload ratio can be defined by application requirement.

4.1.4 Selecting the Current Sensing Resistor (R_S)

The peak value sensed by the 12-bit ADC can be calculated with Equation (16):

$$V_{CSpk\_ADC12} = V_{CSP\_BIAS} + I_{Lpk\_OL} \cdot R_{CS} \quad (16)$$

The reference of 12-bit ADC is 1.6V. Considering a de-rating of 30%, the value of R_s can be calculated with Equation (17):

$$R_{CS} = \frac{(V_{ref\_ADC12} - V_{CSP\_BIAS})}{Ratio_{OL} \cdot I_{Lpk}} \cdot 0.7 \quad (17)$$

Based on this formula, a proper R_S value based on the output power can be selected from the curve shown in Figure 19.

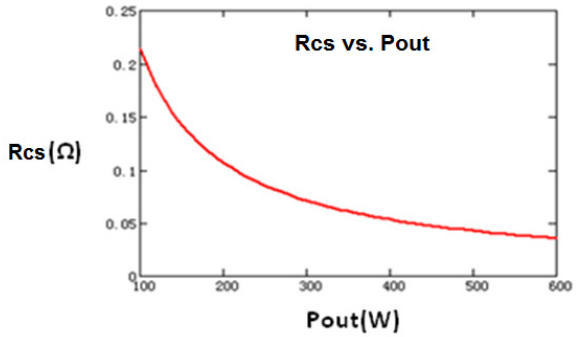
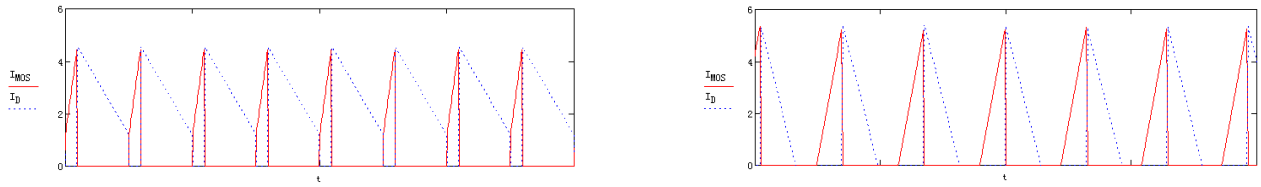


Figure 19: Curve of Relationship between R_{CS} and Output Power

4.1.5 Current of the MOSFET and Diode

Figure 20 shows the waveform of the MOSFET and diode in CCM and DCM.



a) CCM **b) DCM**

Figure 20: Current Waveform of the MOSFET and Diode

The valley current in CCM can be calculated with Equation (18):

$$I_{valley}(V_{in},t) = I_{ref}(V_{in},t) - \frac{\Delta i_L(V_{in},t)}{2} \quad (18)$$

The valley current is zero in DCM operation.
If a switching cycle is treated as an independent waveform, then there can be hundreds of switching cycles in a line cycle. Assume n is the nth switching cycle in a line cycle. The current valley can be calculated with Equation (19):

$$I_{valley}(V_{in},n) = I_{ref}(V_{in},n) - \frac{\Delta i_L(V_{in},n)}{2} \quad (19)$$

The RMS current of the MOSFET of the nth switching cycle can be calculated with Equation (20):

$$I_{MOSRMS}(V_{in},n) = \sqrt{2 \cdot f_{line} \cdot \int_o^{Ton(V_{in},n)} \left(I_{valley}(V_{in},n) + \frac{Vin(n)}{L} \cdot t \right)^2 \cdot dt} \quad (20)$$

Therefore, the RMS current of the MOSFET can be calculated with Equation (21):

$$I_{MOSRMS}(V_{in}) = \sqrt{\sum_{n=1}^{Num} I_{MOSRMS}^2(V_{in},n)} \quad (21)$$

Where Num is the total numbers of switching cycles in a line cycle. In CCM, $Num = f_{sw} / f_{line}$.

Similarly, the RMS current of the diode can be calculated with Equation (22) and Equation (23):

$$I_{DRMS}(V_{in},n) = \sqrt{2 \cdot f_{line} \cdot \int_o^{Toff(V_{in},n)} (I_{valley}(V_{in},n) + \frac{(Vo - Vin(n))}{L} \cdot t)^2 \cdot dt} \quad (22)$$

$$I_{DRMS}(V_{in}) = \sqrt{\sum_{n=1}^{Num} I_{DRMS}^2(V_{in},n)} \quad (23)$$

The peak current of the MOSFET and the diode is the same as the PFC inductor.

4.2 Digital PI Compensator

The HR1211 uses a digital PI to compensate for the voltage loop (see Figure21).

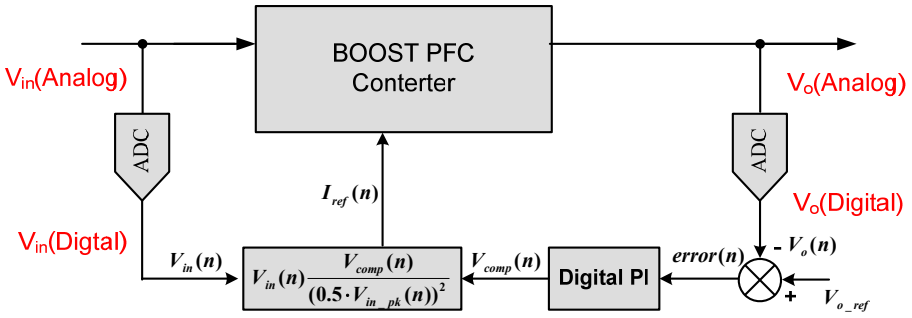


Figure 21: Voltage Compensation Loop

The reference current at AC peak point can be calculated with Equation (24):

$$I_{ref\_pk}(D) = V_{in\_pk}(n) \frac{Vcomp(n)}{(0.5 \cdot V_{in\_pk}(n))^2} = \frac{Vcomp(n)}{0.25 \cdot V_{in\_pk}(n)} \quad (24)$$

The relationship between the input average current and the IC reference current is shown in Equation (25):

$$I_{in\_rms}(A)=\frac{I_{L\_ave}(A)}{\sqrt{2}}=\frac{I_{ref\_pk}(D)}{\sqrt{2}}\cdot\frac{1.6}{1023}\cdot\frac{1}{Rcs}=\frac{Vcomp(n)}{\sqrt{2}\cdot 0.25\cdot V_{in\_pk}(n)}\cdot\frac{1.6}{1023}\cdot\frac{1}{Rcs} \quad (25)$$

The sensed input voltage peak can be calculated with Equation (26):

$$V_{in\_pk}(n)=0.0032\cdot\sqrt{2}\cdot V_{in\_rms}(A)\cdot\frac{1023}{1.6} \quad (26)$$

The sensed output voltage can be calculated with Equation (27):

$$V_o(n)=0.0032\cdot V_o(A)\cdot\frac{1023}{1.6} \quad (27)$$

Based on the energy balance equation shown in Equation (28):

$$I_{in\_rms}(A)\cdot V_{in\_rms}(A)=V_o(A)\cdot I_o \quad (28)$$

Equation (29) can be used to obtain V_{COMP}(n):

$$\frac{Vcomp(n)}{0.5}\cdot\frac{1.6}{1023}\cdot\frac{1}{Rcs}=V_o(n)\cdot I_o \quad (29)$$

Therefore, the transfer function voltage control loop without PI can be calculated with Equation (30):

$$G_{vc}(S)=\frac{dV_o(n)}{dVcomp(n)}=\frac{1.6}{1023\cdot 0.5\cdot Rcs\cdot V_o\cdot C_o\cdot s} \quad (30)$$

A PI regulator in an S domain can be presented with Equation (31):

$$G_{ea}(s)=\frac{K_p\left(s+K_i\right)}{s} \quad (31)$$

For a digital PI, the voltage error can be calculated with Equation (32):

$$error(n)=V_{o\_ref}-V_o(n) \quad (32)$$

The output of the digital PI can be calculated with Equation (33):

$$Vcomp(n)=Vcomp(n-1)+K_P\cdot(error(n)-error(n-1))+K_i\cdot error(n) \quad (33)$$

Therefore, the open loop transfer function can be calculated with Equation (34):

$$G_T(s)=G_{VC}(s)+G_{EA}(S) \quad (34)$$

Base on the above formulas, the Bode plot of G_{VC}(s), G_{EA}(s), and G_T(s) can be calculated and plotted (see Figure 22).

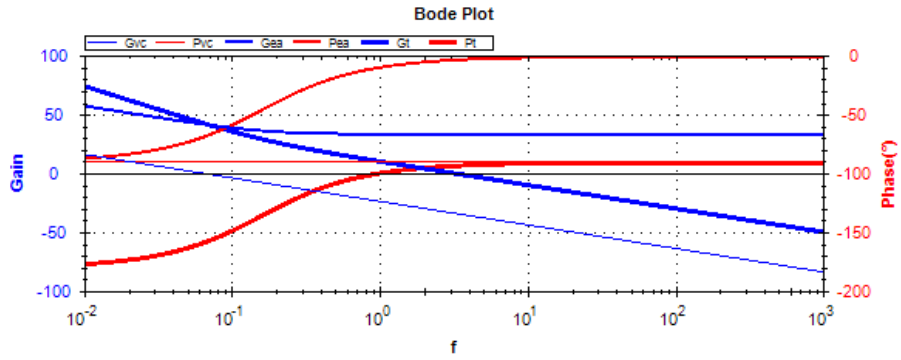


Figure 22: Open Loop Bode Plot

Generally, the cross-over frequency of the PFC is designed to be less than 20Hz. Properly select values for Kp and Ki to get a proper feedback loop performance.

During load dynamics, HR1211 implements fast-loop function to achieve a fast loop response. If the PFC output voltage decreases to the low level voltage of fast loop threshold, or PFC output voltage increases to the high level voltage of fast loop threshold, Ki and Kp will be switched to the programmed fast loop value. In this way, the PFC has a faster dynamic loop response, allowing it to regulate the output voltage to the target value faster.

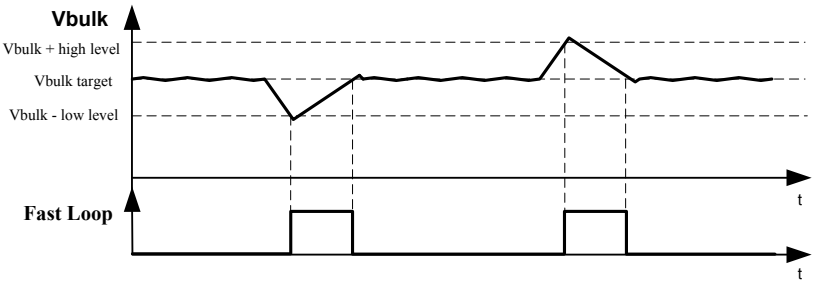


Figure 23: Fast Loop Function

4.3 PFC output Regulation

The PFC output voltage V_{BUS} is regulated by the digital PI loop. If the accuracy of R_{OUT1} and R_{OUT2} in Figure 13 is 1%, the accuracy of V_{BUS} is within 2.5%, considering the accuracy of ADC is about 0.6%.

To optimize the efficiency of the PFC, the HR1211 can auto-adjust the output voltage at different input voltage and output load conditions. For example, the output voltage can be set to be lower when the input voltage is lower. Figure 24 shows how to configure some parameters.

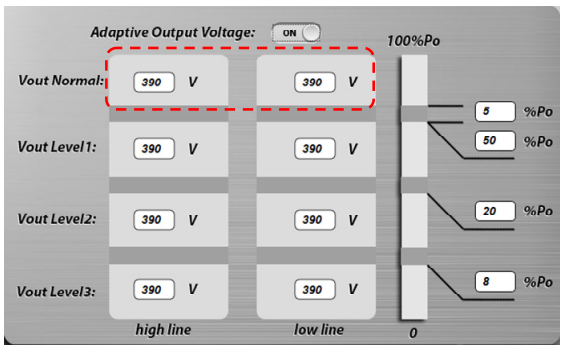


Figure 24: GUI Interface of Output Voltage Regulation

There are a total of eight output voltages that can be programmed. The two columns are determined by the input voltage ranges, which are indicated as high line and low line. The four rows are determined by four output power ranges, and each range can be programmed based on the percentage of the full output power ($V_{COMPFull}$). The relationship of $V_{COMPFull}$ and the full output power is shown in Equation (35):

$$Vcomp_{Full} = 0.0032 \cdot \left(\frac{1023}{1.6}\right)^2 \cdot 0.5 \cdot Rcs \cdot P_{OUT\_Full} \quad (35)$$

The function of the auto-adjustable output can be enabled by setting the Adaptive Output Voltage button to ON; the auto-adjustable output can be disabled by setting the Adaptive Output Voltage button to OFF. Please note that V_{BUS} can be adjusted according to the low line and high line when the adaptive output voltage is off. The target-regulated voltage is programmable by the row marked in the red frame.

4.4 Burst Operation of the PFC

When the output load is decreasing, the PFC converter runs in burst mode operation. The level to enter burst mode is programmable and is set using the percentage of $V_{COMPFull}$. Figure 25 shows the GUI interface of the specific load point needed to enter burst mode. A different burst point can be set at low line and high line.

Figure 25: GUI Interface of Setting Burst Point

The IC stops switching when the load is reducing, if the digital value (V_{COMP}) decreases to V_{COMP_Burst} and V_{BUS} increases to V_{bus_target} plus V_{burst_hys}. The default value of $V_{burst-hys}$ is 5V. If V_{BUS} drops down to $V_{bus-target}$, the IC is enabled and prepare to turn on the gate driver again. Generally, the gate driver only recovers at the peak point of AC line to reduce current stress. Additionally, a threshold voltage $V_{bus-limit}$ that can be programmed is selectable to prevent the bus voltage from dropping too low under transient conditions. This burst behavior is shown in Figure 26.

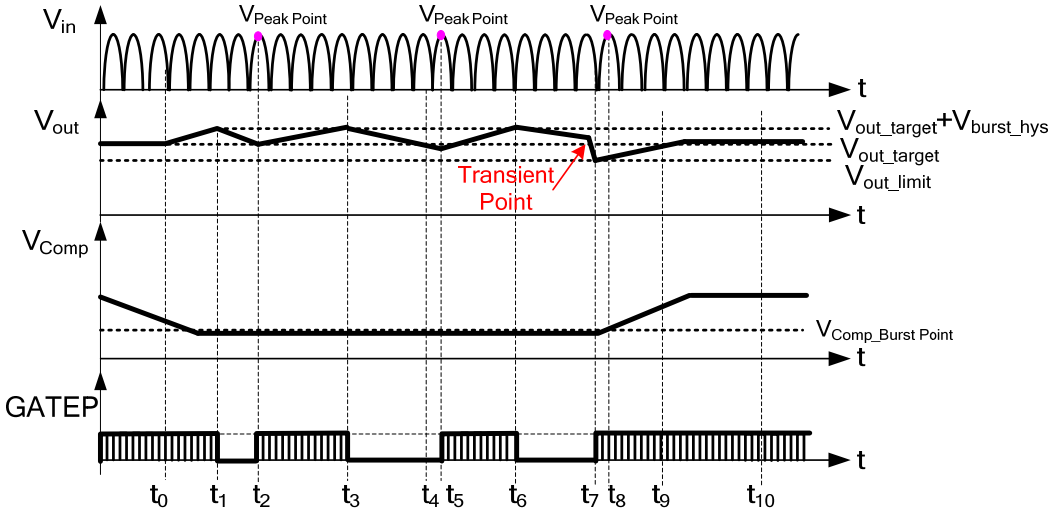


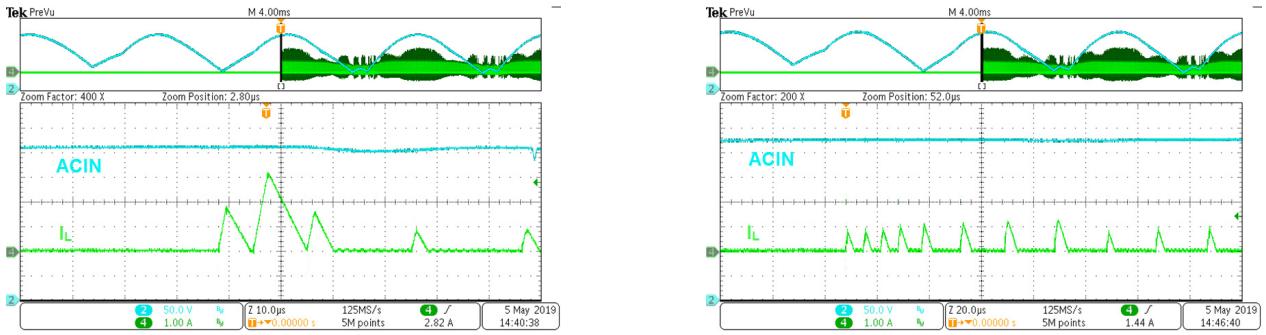
Figure 26: Behavior of PFC Burst Operation

When PFC recovers switching, the first switching cycle always works in CCM due to I_{pk}=0, $I_{pk}(n) < 2I_{ref}(n)$. Thus, he first several CCM switching leads to high peak current which aggravates the

audible noise, as shown in Figure 27-a. HR1211 implements soft switching function at burst recovery to limit the turn-on time and increase the time step by step, as shown in Figure 27-b. The Soft Switching Turn-on Time Limit varies according to different AC input. In low line of input voltage, the pulse on-time is limited with programmed value, and increases with a delta time step by step. In high line of input voltage, the pulse on-time is limited with minimum on-time, and increases with the delta time step by step. The soft switching function does not end until the next on-time is calculated less than the previous one, or the soft turn-on switch number is counted to programmed value (see Table 2). If this function is unnecessary, set the PFC Soft Turn-on Switching Number to zero.

Table 2: Parameters of PFC Burst-out Soft Switching Function

PFC Burst-out Soft Switch		
item	**value**	**unit**
PFC Soft Switching turn-on time Limit	3	us
PFC Soft switch on delta time	80	ns
PFC Soft Turn-on Switch Number	15	cycles



a) PFC Burst-out Soft Switching Function disable

b) PFC Burst-out Soft Switching Function enable

Figure 27: PFC Burst-out Waveforms

4.5 Soft Start of PFC

The HR1211 adopted a PFC soft-start to reduce the current stress at start-up. Figure 28 shows the programmable soft-start time of the PFC. A different soft-start time can be set at low-line voltage and high-line voltage.

Figure 28: GUI Interface of Setting Soft-Start Time

The soft-start time is defined by the internal output voltage reference ramp-up time duration, which is the peak of the input voltage to the target output voltage (see Figure 29).

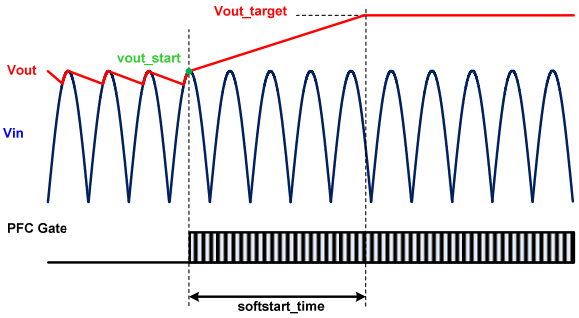


Figure 29: Definition of Soft-Start Time

4.6 Protections

The PFC of the HR1211 provides multiple protection features, such as brown-in and brown-out, over-current limit (OCL), over-voltage protection (OVP) and open-loop protection (OLP). These protection parameters can be programmed by the GUI. Figure 30 shows the GUI interface for setting the protection parameters.

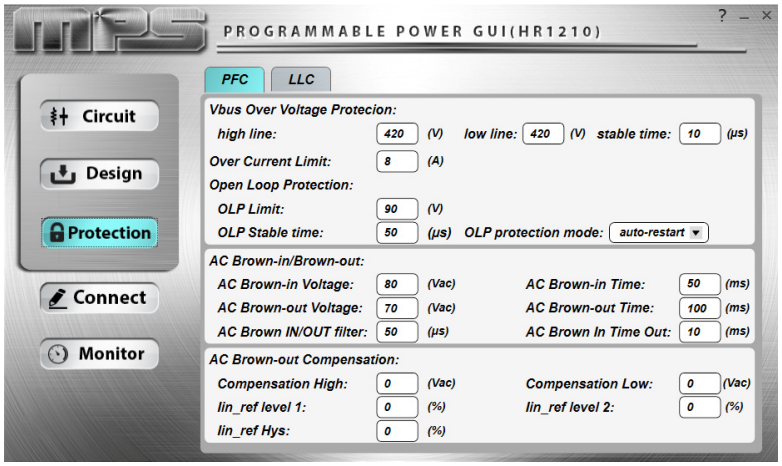


Figure 30: GUI Interface to Set Protection Parameters

4.6.1 AC Brown-In/Brown-Out

To prevent the PFC power devices overstress at a low AC input voltage, HR1211 employs an AC Brown-in/Brown-out function. IC starts operating when input voltage is detected higher than **AC Brown-in Voltage** and shuts down when input voltage is lower than **AC Brown-out Voltage**. **AC Brown-out Voltage** should be set smaller than **AC Brown-in Voltage**.

Since input voltage is a sine wave, input voltage is not always higher than brown-in threshold. **AC Brown-in Time Out** is used to reset the time counter if there is no signal of brown-in comparator output during a fixed time. **AC Brown-in Time Out** must be set longer than line cycle.

HR1211 has two stage Brown-out function. A higher voltage level brown out with a long time can provide enough hold-up time when a slight AC drop. A lower voltage level brown out with a short time can prevent the power device suffering overstress when a huge AC drop.

If the accuracy of R_{IN1} and R_{IN2} in Figure 13 is 1%, and the ADC accuracy is about 0.6%, the accuracy of the brown-in/brown-out threshold is within 2.5%.

Considering the voltage drop of the EMI component, the actual brown-out voltage is higher than the programmed threshold at a heavier load. HR1211 compensates for the voltage difference according to the level of input current. As shown in Table 3, there are two programmable the input current levels that used for brown-out voltage compensation is divided into three programmable ranges. **Compensation Voltage at High Load** is used to compensate the voltage when output larger than **High Load Level**, **Compensation Voltage at Low Load** is used to compensate the voltage when output between **High Load Level** and **Low Load Level**. There is no compensation when output lower than **Low Load Level**. If brown-out accuracy is not needed, **Compensation Voltage at High/Low Load** can be set to zero.

Table 3: Parameters of AC Brown-out Level Compensation Function

AC Brown-out Level Compensation		
item	**value**	**unit**
High Load Level	**70**	**%**
Low Load Level	**30**	**%**

Load Hysteresis	**5**	**%**
B/O Compensation Voltage at High Load	**-5**	**Vac**
B/O Compensation Voltage at Low Load	**-2**	**Vac**

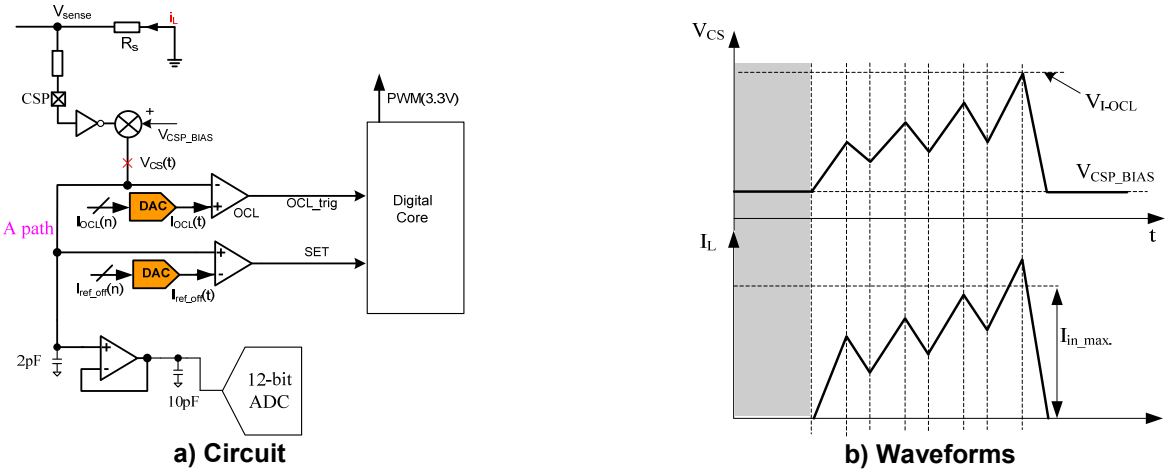
4.6.2 PFC Output OVP

PFC output OVP can be set with different values at low-line voltage and high-line voltage. The PFC stops switching when the output voltage reaches the programmed threshold and resumes switching when the output drops down to the target voltage.

R_{OUT1} and R_{OUT2} can affect the accuracy of the OVP and the 8-bit DAC for OVP. If the accuracy of R_{OUT1} and R_{OUT2} is 1%, the OVP accuracy is within ±2.5%.

4.6.3 PFC Over Current Limit

Figure 31 shows the OCL circuits and waveforms.



a) Circuit **b) Waveforms**

Figure 31: Demonstration of OCL

With OCL, the input power can be limited in over-load condition. This method helps to reduce the risk of over-stress to the power components, therefore improving the robustness of the converter. OCL is achieved cycle by cycle, during which the voltage of V_{CS} is compared to the output voltage (V_{OCL}) of an 8-bit DAC. When V_{CS} is less than V_{OCL}, the PFC gate driver turns off immediately.

4.6.4 PFC Open Loop Protection

If FBP voltage drops below V_{BUS_OLP} for more than the programmable duration, it is considered to be an open-loop condition. The IC will enter into latch or auto-restart protection mode (selectable in GUI) when this condition happens.

If IC is in latch protection mode, the switching is latched off, and can only restart when VCC be charged to above $V_{CCON(HV)}$ after it drops to below V_{CCRST}.

If IC is in auto-restart protection mode, the switching is suspended for an auto-restart timer (can be programmed). If users set “self-power mode” (which means use LLC transformer aux winding to power the VCC), the IC still need to wait for VCC be charged above $V_{CCON(HV)}$ to restart.

4.7 PF Compensation

To meet EMI requirements, an X-cap is usually connected between L and N line, and there is also a high-voltage capacitor connected to the output of the bridge diode is always in parallel with a high-voltage cap. As shown in Figure 32, the input current will be distorted and shift ahead of inductor

current. The current flowing through C_Z (X-cap plus high-voltage cap after bridge) can be calculated with Equation (36):

$$i_{C_Z}(t) = C_Z \frac{dV_{in}(t)}{dt} = 2 \cdot \pi \cdot f_{line} \cdot C_z \cdot \sqrt{2} V_{in\,rms} \cdot \cos(2 \cdot \pi \cdot f_{line} \cdot t) \quad (36)$$

Where f_{line} is the frequency of the input voltage.

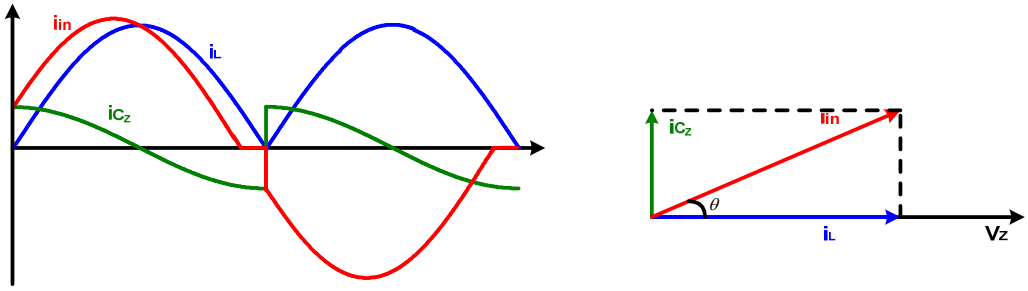


Figure 32: Relationship of Input Current, C1 Current, and Inductor Current

This current causes a phase shift of input current at light load and worsens the power factors and THD. The impact on the PF can be calculated with Equation (37):

$$\cos\theta = \cos\left(\tan^{-1}\left(2 \cdot \pi \cdot f \cdot C_Z \cdot \frac{V_{inrms}^{\ 2}}{P_O}\right)\right) \quad (37)$$

Where P_O is the output power.

Figure 33 shows the influence of C_Z and THD on PF. The larger C_Z is, the lower PF is, particularly at smaller loads. The trend is the same as THD, as a larger THD can deteriorate PF.

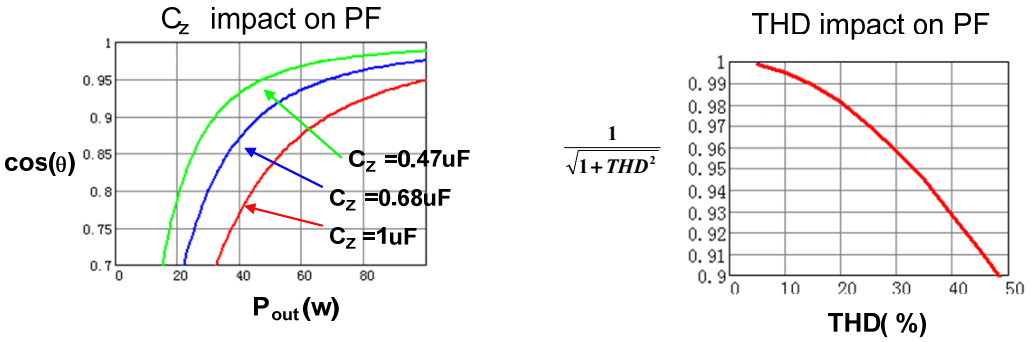


Figure 33: Influence of C_Z on PF and THD

The HR1211 implements a digital triangular wave to compensate for I_{Cz} (see Figure 34).

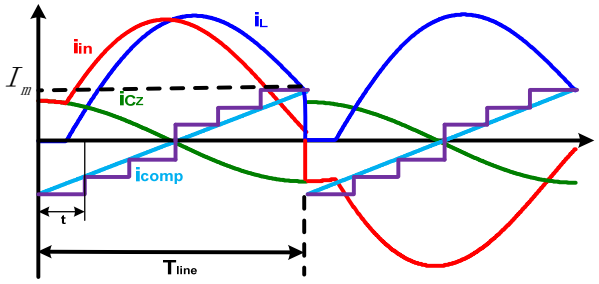


Figure 34: Compensation with Triangular Wave

The amplitude of the triangular wave is calculated based on I_{Cz}, which is determined by the input voltage (V_{IN}), the input capacitor (C_Z), and the line frequency (f_{Line}). In the GUI of the HR1211, compensate the power factor at different values according to the input voltage. There are four input voltage ranges, the typical compensation value is auto calculated with input voltage, input frequency and compensation percentage. So users can set different compensate value at each range (see Figure 35).

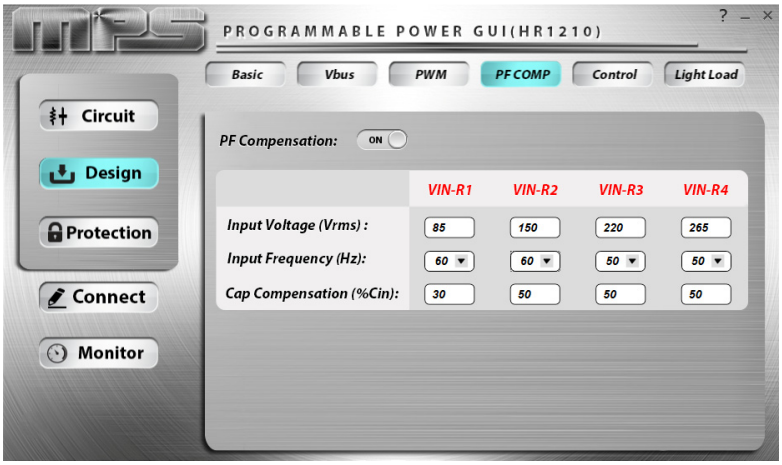


Figure 35: GUI Interface of PF Compensation

The compensation value in VIN-R3 can be calculated with Equation (38):

$$IREF\_COMP\_VALUE = 2 \times \sqrt{2} \times \pi \times Vin(240v) \times Cin(2uF) \times fline(50Hz) \times \%Cin(100\%) \quad (38)$$

Where %Cin is the percentage of the actual capacitance that needs to be compensated.

Figure 36 shows the experimental result of the proposed compensation method of the input capacitor current. PF is improved at high line and light load especially.

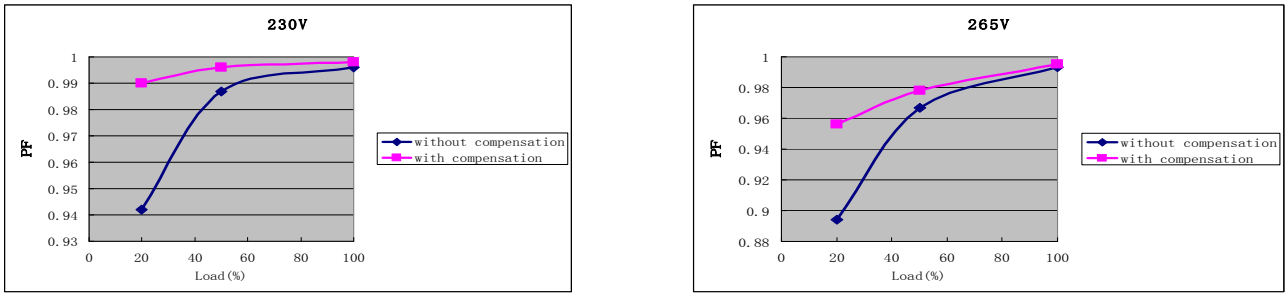


Figure 36: PF Result with and without Compensation Method

4.8 Valley Turn On

In DCM, the HR1211 can turn on at the valley of the MOSFET's drain-to-source switching voltage, which can reduce the switching loss. This function can be enabled or disabled with the HR1211's GUI. This function is enabled when the button reads ON and disabled when the button reads OFF (see Figure 37).

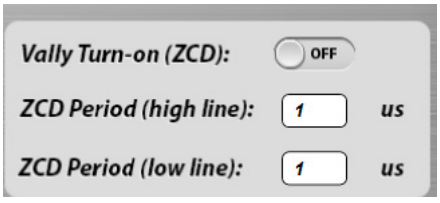
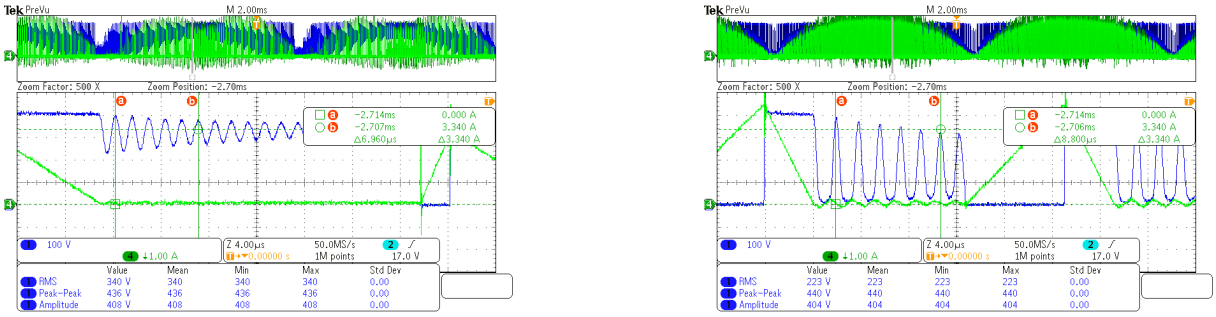


Figure 37: Valley Turn-On GUI Interface

The resonant period at low-line voltage and high-line voltage should be measured respectively and then fill in the GUI interface. Because the resonant period at low line is larger than it is at high line due to the delay time of the body diode recovery. As shown in Figure 38, in five resonant period tests, the time duration at 6.96μs is V_{IN} = 230V, and at 8.8μs is V_{IN} = 110V. Use the average resonant period of high line and low line as the value to fill in the GUI.



a) V_{IN} = 230V b) V_{IN} = 110V

Figure 38: Valley Turn-On GUI Interface

4.9 Frequency Jitter

Frequency jitter is a common method used to pass EMI test. The HR1211 has a frequency jitter function that can be configured by the GUI (see Figure 39). The frequency jitter function is enabled when the button reads ON and disabled when the button reads OFF.

Figure 39: Frequency Jitter GUI Interface

When the jitter function is enabled, the switching frequency of the PFC is modulated around its switching frequency with a variation of programmed amplitude. The frequency modulation can be drawn as a triangle waveform which is shown in Figure 40.

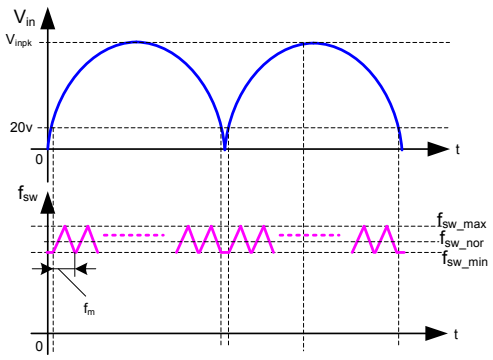


Figure 40: Frequency Jittering

Here, $f_{sw\text{-}max}$ - $f_{sw\text{-}min}$ is the frequency jitter amp and f_m is the jitter modulation frequency.

4.10 Programmable Digital Filter

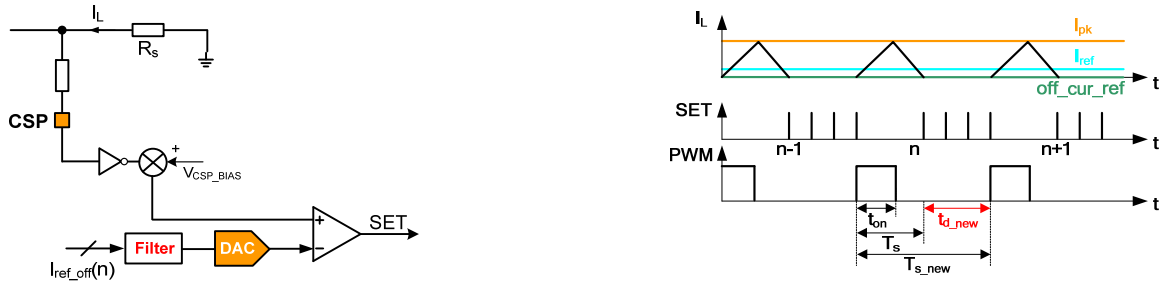
4.10.1 Current Sense Filter

The HR1211 implements two programmable digital filters (csp_filter and td_filter) internally for noisy immunity improvement.

Figure 41-a shows that csp_filter is implemented on the input of the PFC SET comparator. It helps reduce the current distortion and the audible noise in CCM operations. Figure 41-b shows that td_filter is implemented on the calculation of the delay time. It helps reduce the current distortion in DCM operations. With td_filter, the new delay time can be calculated with Equation (39):

$$t_{d\_new}(n) = A \cdot t_d(n) + (1-A) \cdot t_{d\_new}(n-1) \quad (39)$$

Where A is a coefficient related to the bandwidth of td_filter.



a) csp_filter b) td_filter

Figure 41: Programmable Digital Filter

Both csp_filter and td_filter are second-order filter and can be configured by the GUI (see Figure 42). The filter function is enabled when the button set ON and disabled when the button set OFF. There are 15 levels of bandwidth for each order filter which is selected flexibly according to practical applications.

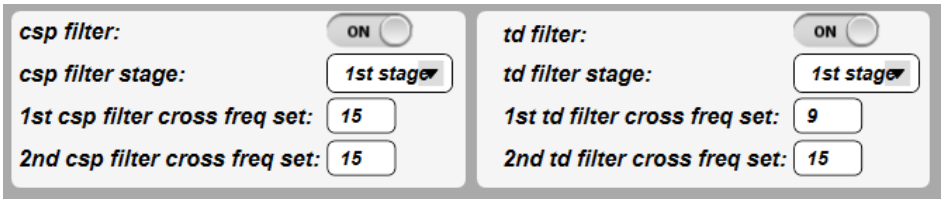


Figure 42: Parameters of Programmable Digital Filter

4.10.2 Voltage Sense Filter

To enhance the anti-interference ability of PFC output voltage sense, HR1211 implements a programmable filter on FBP sensing. The cut-off frequency of the digital filter is programmable with three levels. With the voltage sense filter, the capacitor (C_3) parallel with R_{out2} can be reduced, which can improve the dynamic response and improve the accuracy of overvoltage protection.

5. HB RESONANT FUNCTIONS

The half-bridge resonant converter (LLC) can achieve high efficiency with the benefit of zero voltage switching (ZVS). HR1211 uses a patented current mode control method for LLC converter.

5.1 Current Mode Control

As shown in Figure 43, the voltage mode LLC controller (e.g. HR1001) adjusts the frequency to control the output power based on the first-harmonic approximation (FHA), which describes the relationship between the DC gain (M) of the LLC resonant tank and the switching frequency.

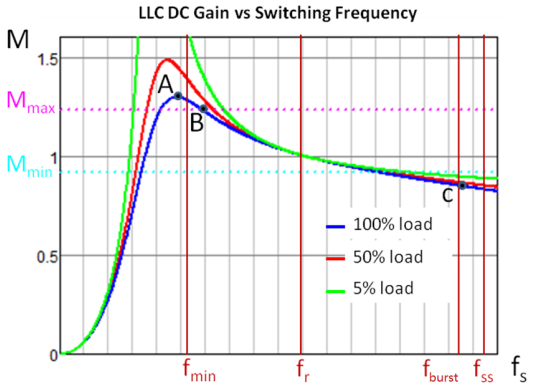


Figure 43: DC Gain of the LLC Converter

HR1211 uses a current mode control method for LLC converter. Equation (40) shows that the output power has a linear relationship with the resonant capacitor voltage difference ΔV_{Cr}. The ΔV_{Cr} has an integral relationship with the resonant current I_r, as shown in Equation (41).

$$P_{out} = \eta \cdot P_{in} = \eta \cdot V_{bus} \cdot \Delta V_{Cr} \cdot C_r \cdot f_s \quad (40)$$

$$\Delta V_{Cr} = \frac{\int_0^{\frac{T}{2}} I_r dt}{C_r} \quad (41)$$

Where T is the switching period.

HR1211 uses an comparator to control the resonant capacitor voltage difference ΔV_{Cr} directly to control the output power. The advantage is that HR1211 obtains a quicker response than a voltage mode controlled system.

Figure 44 shows the control block diagram of the HB LLC. The on-time comparator is used to turn off the high side gate (HG) by comparing the current sense signal (V_{CS}) with the feedback signal (V_{COMP}). The HG on-time is re-used for low side gate (LG). A digital counter with $1/f_{osc\_LLC}$ minimum step is implemented to ensure the on-time matching of HG and LG.

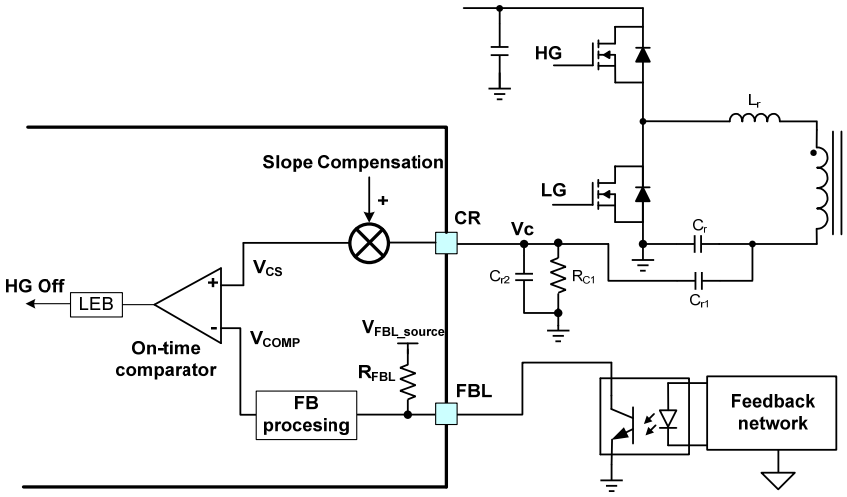


Figure 44: LLC control block diagram

Figure 45 shows the LLC current mode control strategy by sensing CR and FBL voltage which determines the LLC switching frequency.

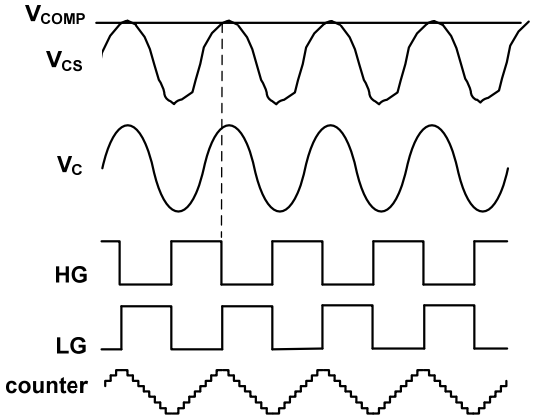


Figure 45: LLC Current Mode Control Strategy

CR pin senses the resonant capacitor Cr voltage by the external cap divider (C_{r1}, C_{r2}). The capacitor division ratio determines the maximum output power (primary current) of the LLC stage. A resistor (R_{c1}) paralleled with C_{r1} is used to eliminate the DC component.

HR1211 senses the voltage of opto-coupler on FBL to generate the reference (V_{COMP}) of the internal on-time comparator which determines the HG on-time. The LG follows the previous HG on-time. There is an internal pull-up resistor R_{FBL} assures that the FBL voltage increases with the output load increasing.

5.2 LLC Operating Mode Control Strategy

For HB LLC topology, the switching frequency gets higher which lead to magnetization and switching losses increase at light load condition. To control the output voltage and limit power consumption, the HR1211 implements a skip mode operation in light load and a burst mode operation in extremely light load which greatly reduces the average switching frequency, thus reducing the magnetic losses.

As shown in Figure 46, there are 3 operation mode: continuous steady state, skip mode and burst mode, which are determined by the FBL pin voltage. When V_{FBL} triggers the threshold (V2), the LLC system enters into skip mode and if FBL voltage further drops (load decrease) to below threshold (V4), LLC switch triggers burst-off and LLC enters burst mode. Both skip mode and burst mode threshold has

a hysteresis V3 & V5, above which the LLC enters back to continuous steady state or skip mode. All the threshold V2-V5 can be programmable in GUI.

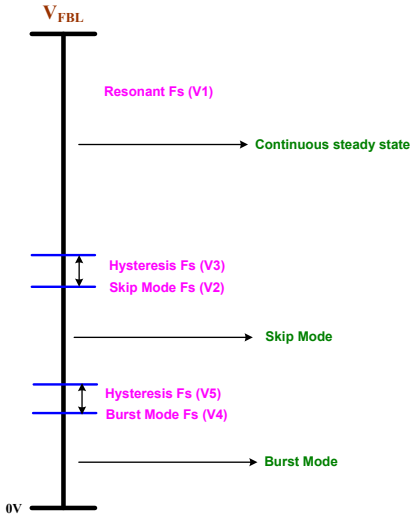


Figure 46: LLC Working Mode by Monitoring FBL

Figure 47 shows the corresponding block diagram for this FBL voltage process and on-time comparator.

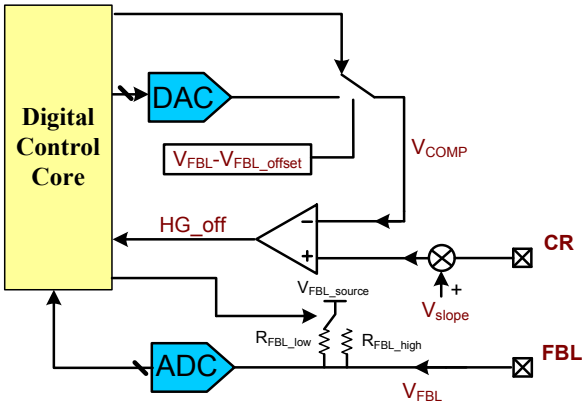


Figure 47: FBL Voltage Processing for on-time Comparator

During continuous steady state mode, the FBL voltage is used as the reference for the on-time comparator by Equation (42):

$$V_{COMP} = V_{FBL} - V_{FBL\_offset} \quad (42)$$

During skip mode & burst mode, the sampled FBL voltage is internally processed to V_{COMP} by digital core and output from a 10-bit DAC which used as reference for the on-time comparator for turn-off the HG gate driver, the 10-bit DAC output is calculated with Equation (43):

$$V_{COMP} = A \cdot V_{FBL} + B \quad (43)$$

Where **A** is the proportional coefficient and **B** is an offset for V_{COMP} which both can be set in GUI.

Figure 48 shows the relationship of V_{COMP} and FBL voltage.

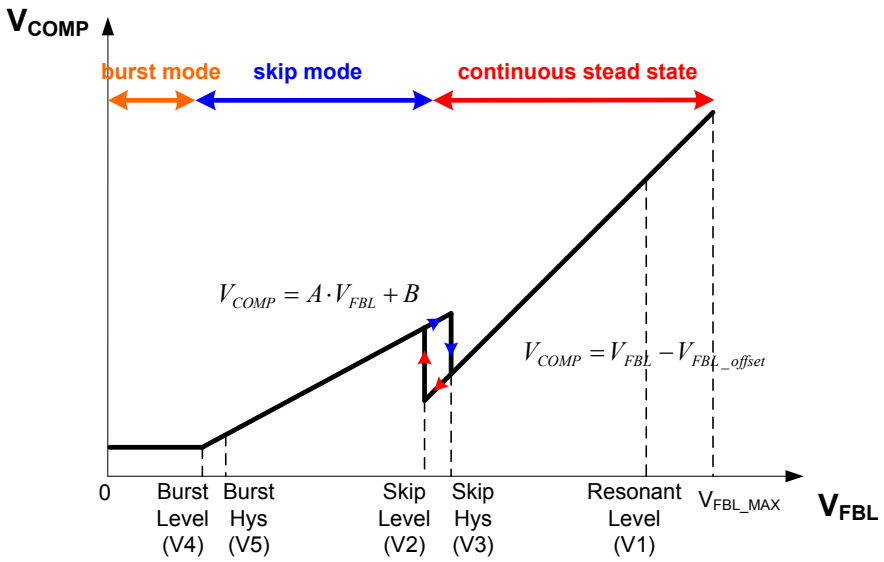


Figure 48: V_{COMP} - V_{FBL} Curve

5.2.1 Skip Mode Operation

When system enters skip mode, a switch-idle (both HG and LG) period will be implemented every N (programmable in GUI) switching cycles. The skip cycle frequency f_{skip} is kept at a programmable value. The 1st high side gate always turns on with ZVS condition to minimize the switching loss (see Figure 49).

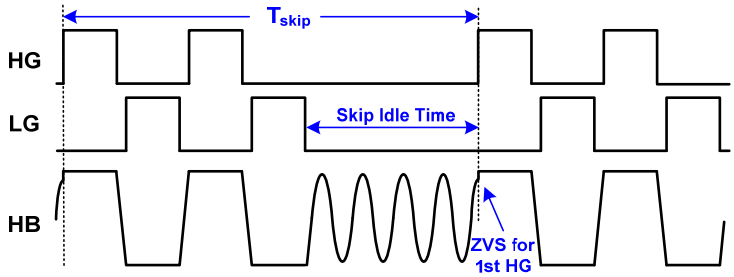


Figure 49: Skip mode operation of LLC

Figure 50 shows the GUI interface of skip mode parameters.

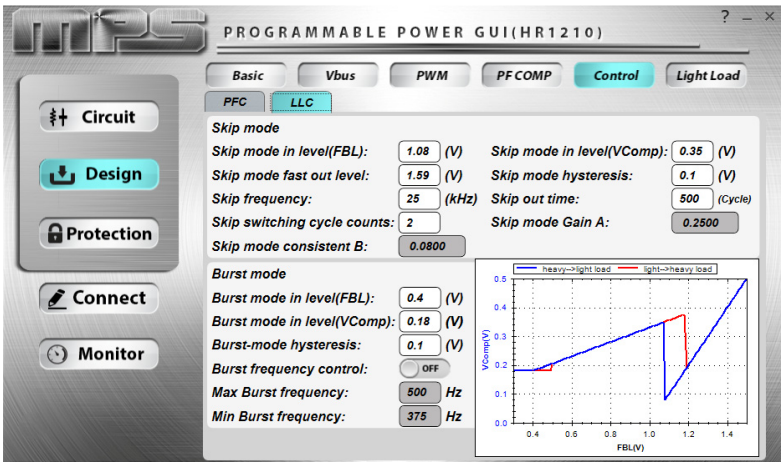


Figure 50: GUI interface of skip mode

Skip mode in level(FB) is the FBL voltage which is the threshold (V2) of entering skip mode. E.g. skip mode is required under 20% load. The approximate value of **Skip mode in level(FB)** can be calculated with Equation (44):

$$\text{Skip mode in level(FB)} \approx 20\% \cdot (V_{FBL\_full} - V_{FBL\_offset}) + V_{FBL\_offset} \quad (44)$$

Where V_{FBL_full} is the voltage of FBL in the full load.

Skip mode in level(Ref) is the output of 10-bit DAC when FBL voltage is the value of **Skip mode in level(FB)**. The **Skip mode in level(Ref)** should be larger than Equation (45), otherwise the output power in skip mode cannot sustain the output, which leads the bounce between the skip mode and continuous steady state mode.

$$\text{Skip mode in level(Ref)} > \frac{f_S}{N_{skip} \cdot f_{skip}} \cdot (\text{Skip mode in level(FB)} - V_{FBL\_offset}) \quad (45)$$

Where f_s is the switching frequency in skip mode, N_{skip} is the **Skip switching cycle counts**, f_{skip} is the **Skip frequency**. The value calculated by Equation (45) is only used for reference, it also needs to be fine-tuned according to the actual operating conditions.

In case of oscillation when IC translates from the continuous steady state mode to skip mode, the 1st skip mode cycle works after a delay of a programmable continuous cycles (see figure 51).

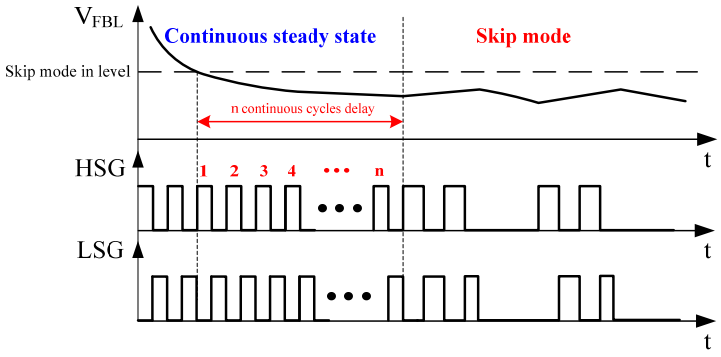
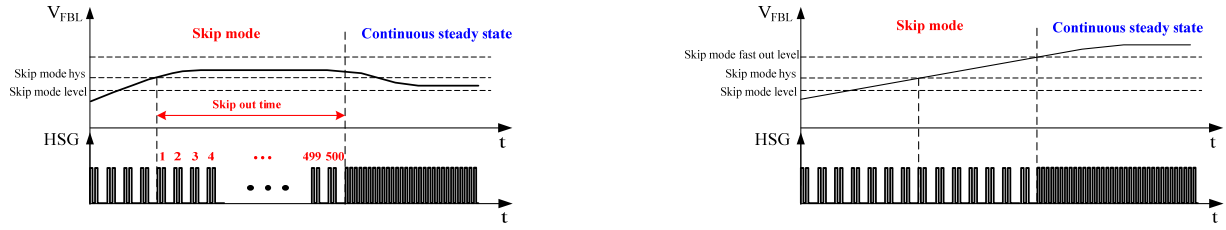


Figure 51: Waveform of conversion from steady state mode to skip mode

Once HR1211 entries the skip mode, the **Skip mode hysteresis** and **Skip out time** ensure that operation mode does not bounce between the steady state mode and skip mode. The value of **Skip out time** in the GUI is the number of skip mode cycles. E.g. setting the **Skip out time** to 500, When the FBL voltage trigger the skip mode threshold plus the skip mode hysteresis, HR1211 converts from skip mode to steady state mode after 500 skip mode cycles (see Figure 52-a). The **skip mode fast out level** is used to entry steady state mode directly in the dynamic conditions in case of the excessive voltage drop of output (see Figure 52-b).



a) Skip out time delay waveform **b) Skip mode fast out waveform**

Figure 52: Waveform of conversion from skip mode to steady state mode

5.2.2 Burst Mode Operation

As the load gets even lighter, to further limit the average switching frequency, a longer switch idle time will be inserted into the skip mode, which is called burst-mode operation.

As shown in Figure 53, during burst-on period, the LLC works in skip-mode which describes in Figure 48. During burst-off, the switching is totally off, the burst-off period ends when the FBL voltage increases to trigger V_{B_ON} threshold (programmable).

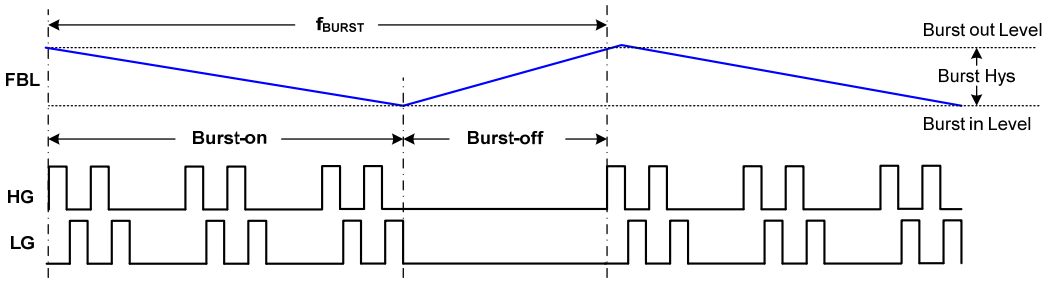


Figure 53: Burst mode operation of LLC

The burst frequency f_{BURST} can be adjusted by increasing or decreasing the switching pulses during burst-on period. By adjusting the burst frequency to a proper range, the audible noise during burst mode can be greatly decreased. As shown in Table 4, the Max Burst Frequency is the target of frequency control. If the burst frequency is between the range of Max/Min Burst Frequency, HR1211 keeps the current state. Burst Frequency Blanking Period is used to blank several burst cycles to wait the system stable, then enable next frequency control.

Table 4: Parameters of LLC Burst Frequency Control

LLC Burst Frequency Control		
item	**value**	**unit**
Burst frequency control enable	**1**	
Max Burst Frequency	**500**	**Hz**
Min Burst Frequency	**400**	**Hz**
Burst Frequency Blanking Period (Burst cycles)	**3**	

Figure 54 shows the burst frequency control strategy waveforms. E.g. the current burst frequency $f_{burst}[0]$ is 1000Hz, the pulse cycles counter N[0]=4, the target control frequency is 500Hz, thus, HR1211 calculates the pulse number N[1] of next burst cycle to control the frequency with Equation (46):

$$N[1] = \frac{N[0] \cdot f_{burst}[0]}{f_{\text{target}}} \quad (46)$$

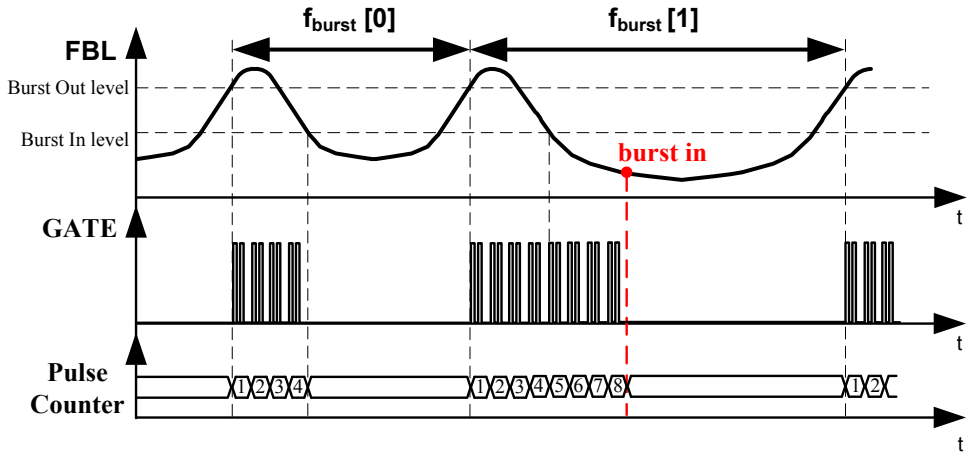


Figure 54: Burst Frequency Control Strategy

Where f_{target} is the Max Burst Frequency programmed by user. If the next burst frequency f_{burst}[1] is between Max Burst Frequency and Min Burst Frequency, HR1211 will not change the next pulse cycles.

During the deep burst mode operation, the burst-off time is so long that the BST capacitor voltage drops too low. Therefore, LG is turned on first for a programmable time when enter into burst-on if the burst-off time exceeds the timer set in GUI to charge the BST voltage. E.g. as shown in Figure 55, if the burst-off time is longer than 80ms (**Bootstrap cap discharge Time**), the LG is turned on first for 80us (**First low-side gate on Time**) when IC exits the burst mode. Due to the long time LG turn-on, adaptive dead-time adjustment (ADTA) is ineffective, an **Idle time after 1st low-side gate** is used to prevent shoot-through.

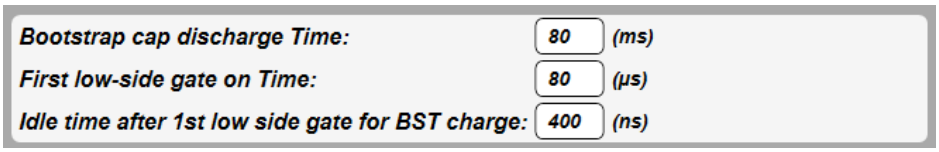


Figure 55: GUI interface of first LSG on function in bust mode

5.2.2.1 Power Saving on Feedback Loop

In deep burst mode (the switching counts during one burst-on period is lower than a programmable value), the FBL pull up resistor R_{FBL} is increased from R_{FBL_low} to R_{FBL_high} gradually (with a programmable timer) to decrease opto current to save power loss.

As shown in Figure 56, the **Pulse Counts**, **Stable Time** and **Exit Time** is the criterion of switching FBL-pull resistor. If the number of skip cycles in one burst cycle is less than **Pulse Counts** for the programmed consecutive burst cycles (**Stable time**), HR1211 switches FBL pull-up resistor from R_{FBL_low} to R_{FBL_high}. Once IC switches to R_{FBL_high}, If the number of skip cycles in one burst cycle is larger than **Pulse Counts** for **Exit time**, HR1211 switches FBL pull-up resistor to R_{FBL_low}. HR1211 is added a programmable hysteresis of **Pulse counts** to keep the power save function stable.

To prevent the loop oscillation of switching FBL pull-up resistor, a translation time of each switching direction can be set. A basic time should be guaranteed, and a long addition time can be set independently of each switching direction. E.g. setting the basic time as 100ms, setting the addition time of R_{FBL_low} to R_{FBL_high} as 2x256ms, and setting the addition time of R_{FBL_high} to R_{FBL_low} as 1x256ms. So the total translation time of R_{FBL_low} to R_{FBL_high} is 612ms, and the total translation time of R_{FBL_high} to R_{FBL_low} is 356ms.

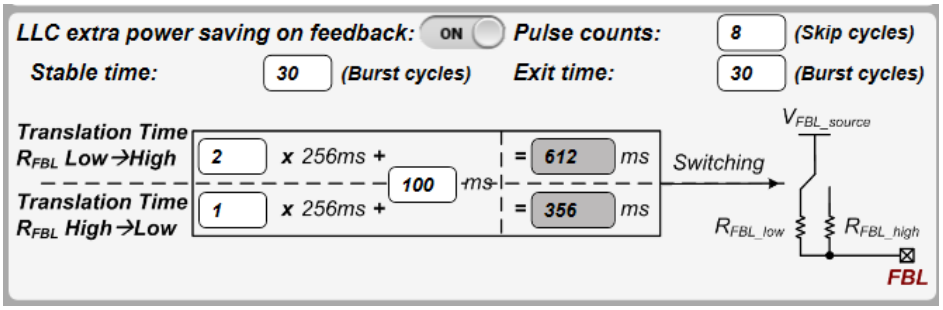


Figure 56: GUI interface of Switching FBL Pull-up Resistor

5.2.2.2 Ultra Low Power Mode

In order to further reduce the IC power consumption, HR1211 implements ultra low power mode during burst-off period (both PFC and LLC enter burst mode). In ultra low power mode, the system clock is reduced to 1/10, some internal bias current shuts down. The total IC consumption is reduced to I_{CC_Brust} (typically 1.8mA).

As shown in Figure 57, HR1211 entries the ultra low power mode when PFC and LLC burst-off. HR1211 exits ultra low power mode when PFC burst-out or FBL higher than a voltage threshold which is output from a programmable 8-bit DAC. This voltage threshold should be set between burst in and burst out level.

A low voltage threshold (need lower than burst in level) is set to force HR1211 suspending LLC switching and entering ultra low power mode, if PFC is burst off. This threshold is used to prevent the output overshoot in load dynamic condition or LLC burst frequency control. Since the ultra low power mode in level suspends the switching, the LLC burst frequency control will be interrupted, thus burst frequency will be higher than target. If users prefer burst frequency and don't care about the output overshoot, a force burst frequency control switch function can be set.

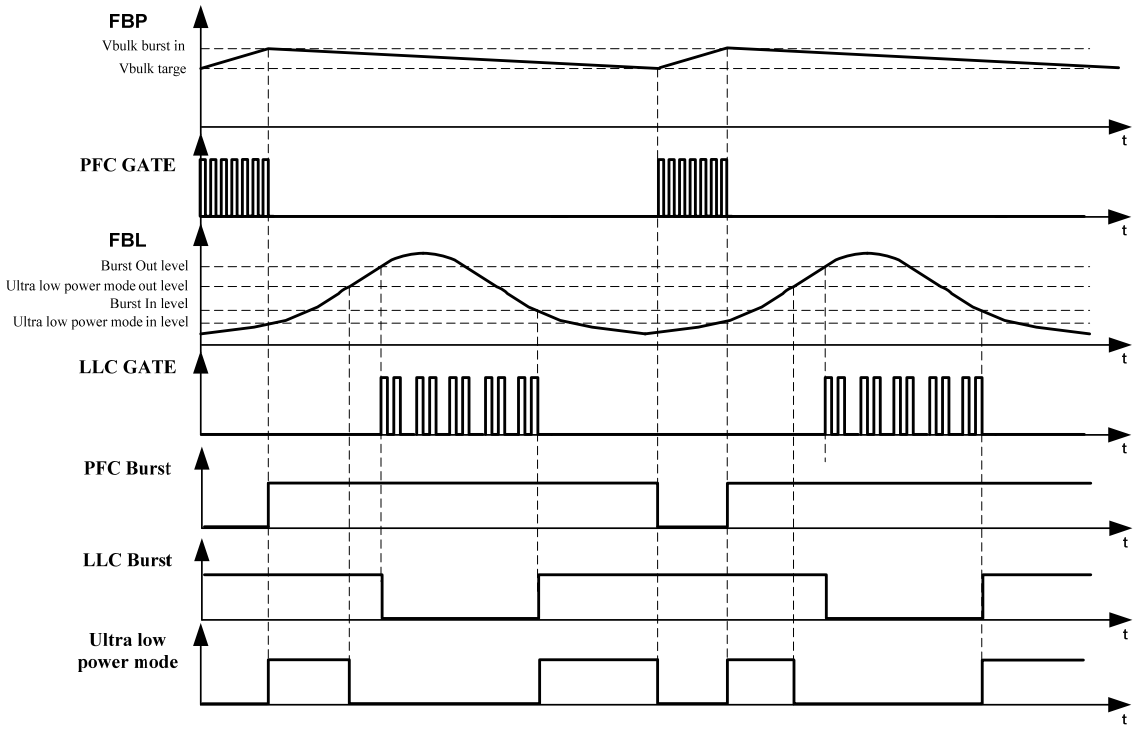


Figure 57: Ultra Low Power Mode

5.3 Enabling and Disabling LLC Operations

As described in the IC power management section and shown with the waveforms in Figure 4, if VCC and VREG are normal, then the LLC is enabled when D2D_BI/BO is high, which indicates that the PFC output voltage is larger than the LLC brown-in threshold. The LLC is disabled when D2D_BI/BO is low, which indicates that the PFC output voltage has dropped below the LLC brown-out threshold.

The brown-in threshold and brown-out threshold of the LLC can be set (see Table 5). **LLC Brown-in after PFC Brown-in** switch is used to suspend LLC working until PFC enable, otherwise, LLC and PFC enable independently.

Table 5: Parameters of LLC Brown-in/out

LLC Brown-in/Brown-out		
item	**value**	**unit**
LLC Brown-in after PFC Brown-in	**1**	
LLC Brown-in Voltage	**380**	**V**
LLC BI Timer (FB sample count)	**15**	
LLC Brown-out Voltage	**340**	**V**
LLC Brown-out Timer	**200**	**us**

5.3 Soft start Operation

During LLC switching start-up, the internal V_{COMP} is overridden by a soft-start generator output voltage. The soft-start timer can be set in GUI to define the soft-start duration.

At the beginning of startup, LG will be turned on first for a programmable time to charge up the BST cap voltage (see Figure 58).

Because of resonant cap Cr voltage imbalance during system start-up, the current slew rate in the resonant tank has a significant difference when HG and LG gate driver turned on. With 50% duty cycle of HG and LG gate driven, the resonant tank current may not reverse in a switching half-cycle, in which condition hard switching may occur (see Figure 58). In HR1211, the LG gate driver will not be turned off until the resonant tank current drops below zero (V_{CSHB}<V_{CSNR}) to avoid hard switching during soft-start.

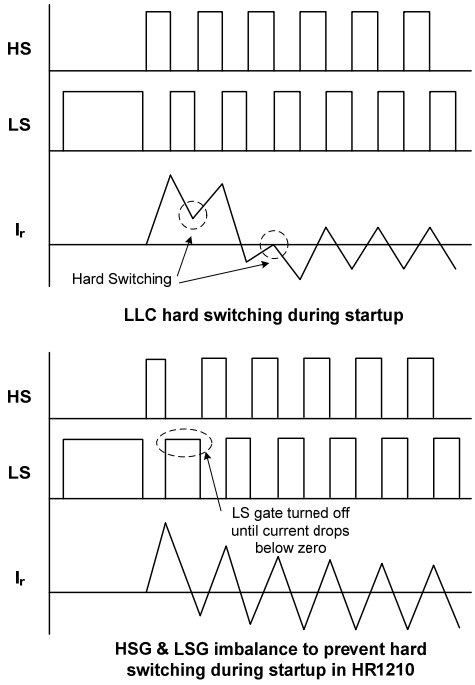


Figure 58: LLC start-up to avoid hard switching in HR1211

5.4 Adaptive Dead-Time Adjustment (ADTA)

The adaptive dead-time control function adjusts the dead time automatically, which allows the LLC converter to achieve high efficiency from light load to full load due to ZVS.

Figure 59 illustrates the possible dead time with ADTA logic. Note that there are three possible dead time, minimum dead time (t_{DMIN}), Maximum dead time (t_{DMAX}), and adjusted dead time which value is between t_{DMIN} and t_{DMAX}. When the transition time of SW is smaller than t_{DMIN}, the logic prevents the gate of HG or LG until t_{DMIN} is reached. This can avoid any shoot-through of the high-side and low-side MOSFET. If the dead time is too long, it may lead to duty cycle loss and loss of soft switching. So a maximum dead time t_{DMAX} is set forcing the gate to switch on. Both t_{DMIN} and t_{DMAX} can be programmable in GUI.

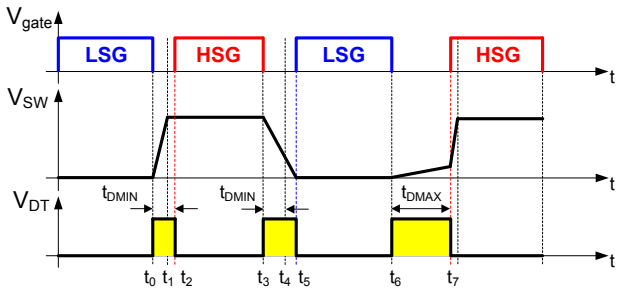


Figure 59: Waveforms Demonstrate ADTA

5.5 Slope Compensation function

For current mode control stability, a digital 4-bits programmable slope voltage V_{CR_Slope} is added on the sensed voltage V_{CR} to generate V_{CS} (see Figure 60).

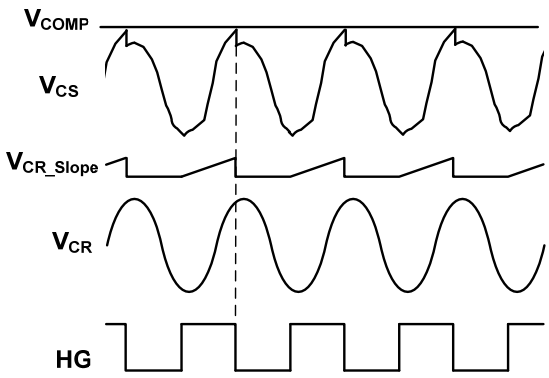


Figure 60: Slope compensation waveform

As shown in Table 6, the slope compensation per LSB is dV_{Slope}/dt (typically 2.6mV/us). E.g. set the **slope compensation level select** to 2, and the HSG turn on time is 5us, thus the compensated voltage on V_{CS} is $2 \cdot 2.6^{mV}/_{us} \cdot 5us = 26mV$.

Table 6: Parameters of LLC Slope Compensation

LLC Slope Compensation		
item	**value**	**unit**
LLC slope compensation level select	**0**	
LLC slope compensation on level	**1.55**	**V**
LLC slope compensation off level	**1.4**	**V**
LLC Slope compensation always on EN	**0**	

The function can also be disabled when output load (FBL voltage) is lower than a programmable threshold, in case the ramp voltage affects the load level of skip in/out and burst in/out. **Slope compensation on level** is used to enable the slope compensation function when the FBL voltage is higher than the threshold. **Slope compensation off level** is used to disable the slope compensation function when the FBL voltage is lower than the threshold. **Slope compensation always on EN** is used to enable the slope compensation function all the time, even if the FBL voltage lower than **Slope compensation off level**.

5.6 Protections

5.6.1 Capacitive Mode Protection (CMP)

In fault conditions like over-load or short circuit, or just load transient condition, the LLC converter may run into capacitive region. In capacitive mode, the voltage applied on resonant tank is lagging off the current, which makes the MOSFETs lose ZVS and even be damaged, so operating in capacitive region should be avoided.

Figure 61 shows the principle of the capacitive mode protection in HR1211. CSPOS and CSNEG stands for the current polarity, which is generated by comparing voltage of CSHB pin with internal V_{CSPR} and V_{CSNR} voltage threshold.

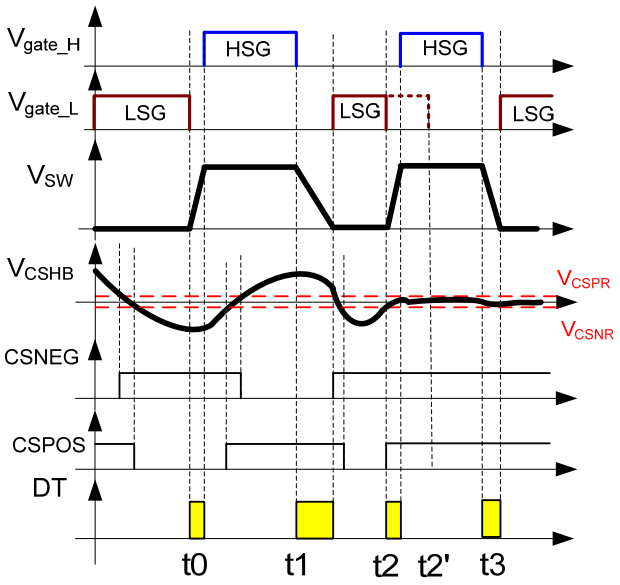


Figure 61: Operating Principle of CMP

At t0, the moment when Low-side gate driver is turned off, V_{CSHB}<V_{CSNR} which means current flows at right polarity (negative), so that convertor is operating in the inductive mode. Capacitive mode protection doesn't take action.

At t1, the moment when High-side gate driver is turned off, V_{CSHB}> V_{CSPR} which also imply current flows at right polarity (positive), so that convertor is operating in the inductive mode. Capacitive mode protection doesn't take action, either.

At t2, V_{CSHB} reaches V_{CSNR}, while the LG turn-off signal still didn't come. In this case, if the system waited for the LG turn-off signal (at t2'), the LLC converter would work in the capacitor mode. In order to avoid this capacitor mode operation, LG will be forced turned off when V_{CSHB} crosses above V_{CSNR}, instead.

If V_{CSHB} never cross above V_{CSPR} during HG on time, the CMP function won't be activated when HG is turning off. Vice versa, if V_{CSHB} never cross below V_{CSNR} during LG on time, the CMP function won't be activated when LG is turning off.

Figure 62 shows the GUI interface of CMP parameters. A CMP function filter is used to prevent the spurious triggering of CMP. The blanking time can be also programmable in the GUI.

Figure 62: GUI interface of CMP

5.6.2 Over Current Protection (OCP)

HR1211 provides the short circuit protection by triggering the V_{CSHB} voltage at V_{CS-OCP}. A **OCP Protection Voltage Level select** switch is used to select the voltage reference of V_{CS-OCP}. If the switch =0, V_{CS-OCP}=2V, If the switch =1, V_{CS-OCP}=1.5V. An internal counter will be incremented each time V_{CS-OCP} is triggered and OCP protection takes action when the counter counts to N which is programmable in GUI and the maximum value is 7. This condition normally happens when the CSHB pin voltage continues to rise during a short circuit. IC can be selected for latch protection mode or auto restart protection mode in GUI when LLC OCP happens (see Figure 63).

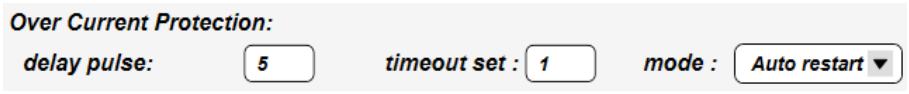


Figure 63: GUI interface of OCP

OCP Timeout Set is used to enhance the sensitivity of OCP. During the HR1211 counting the OCP cycles, it allows the interruption of N cycles (OCP Timeout). The OCP timing sequence is shown in Figure 64. E.g. OCP Delay Pulse is set to 5, OCP Timeout is set to 1.

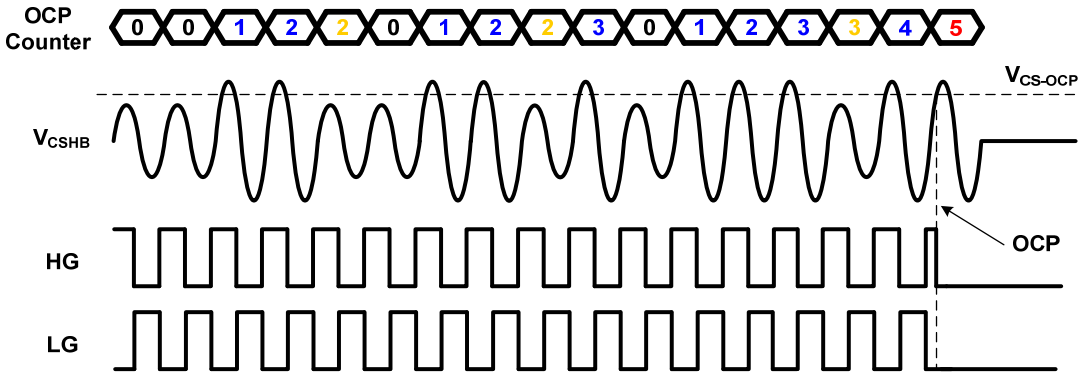


Figure 64: Operation Principle of OCP

5.6.3 Over Power Protection (OPP)

The LLC OPP function is implemented by the detection of FBL pin voltage. The FBL pin voltage is monitored and when the voltage exceeds V_{OPP_LLC} (programmable in GUI), an internal programmable timer is triggered on. This timer is reset when FBL voltage falls below V_{OPP_LLC}. OPP function will be triggered if the timer counts to the end without reset. IC can be selected for latch protection mode or auto restart protection mode in GUI when LLC OPP happens (see Figure 65).

Figure 65: GUI interface of OPP

5.6.4 SO pin Protection

HR1211 monitors the voltage on SO pin and provide a protection function when V_{SO} exceeds V_{SO_OVP} for a programmable timer T_{OVP_stable} (see Figure 66).

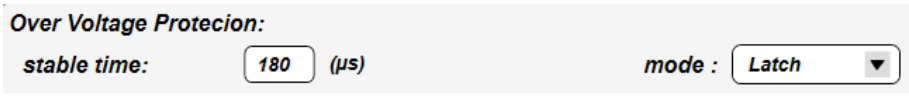


Figure 66: GUI interface of SO pin protection

As shown in Figure 67, the SO pin can be connected to the primary auxiliary winding by a resistor divider to sense the output voltage, which used as over voltage protection (OVP). The voltage on SO pin is calculated with Equation (47):

$$V_{SO} = \frac{R_{SO1}}{R_{SO1} + R_{SO2}} \cdot \frac{N_{PAU}}{N_s} \cdot (V_O + V_{FD}) \quad (47)$$

Where: N_{PAU} is the turns of auxiliary winding

N_S is the turns of secondary winding

V_O is the output voltage and V_{FD} is forward voltage drop of output rectifier or SR.

R_{SO1} and R_{SO2} is the voltage divider for sampling.

An external NTC can also be used on this pin as external OTP function. Pull up SO pin with an NTC resistor to a constant voltage source (VREG etc.), as shown in Figure 67. The pull up resistor RSO2 is to limit the maximum voltage on SO, which is usually ≤3V to avoid SO pin overvoltage. The voltage on SO pin is calculated with Equation (48):

$$V_{SO} = \frac{R_{SO1}}{R_{NTC} + R_{SO1} + R_{SO2}} \cdot V_{REG} \quad (48)$$

Where R_{SO} is the external pull down resistor connect on SO pin to GND.

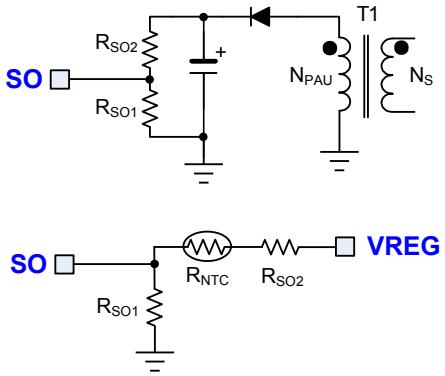


Figure 67: SO Application Circuit for OVP and external OTP Function

5.7 LLC Resonant Tank Parameters Design

The on-line design tool is available in below website:
https://www.monolithicpower.com/en/llc-design-tool

MPS's AN054 details the analysis and design of LLC resonant tank parameters based on HR1000, as shown in below website:
https://www.monolithicpower.com/en/design-tools/application-notes.html

5.8 Sensing Circuit Design

5.8.1 CR Sensing Circuit

As shown in Figure 68, the current sense voltage V_{CR} is derived from the resonant tank capacitor Cr. The voltage on Cr is divided by external cap divider (C_{r1}, C_{r2}) before it is sensed on CR pin. The capacitor division ratio determines the maximum output power (primary current) of the LLC stage. The resistor R_{CR} paralleled with C_{r2} is used to eliminate the DC bias.

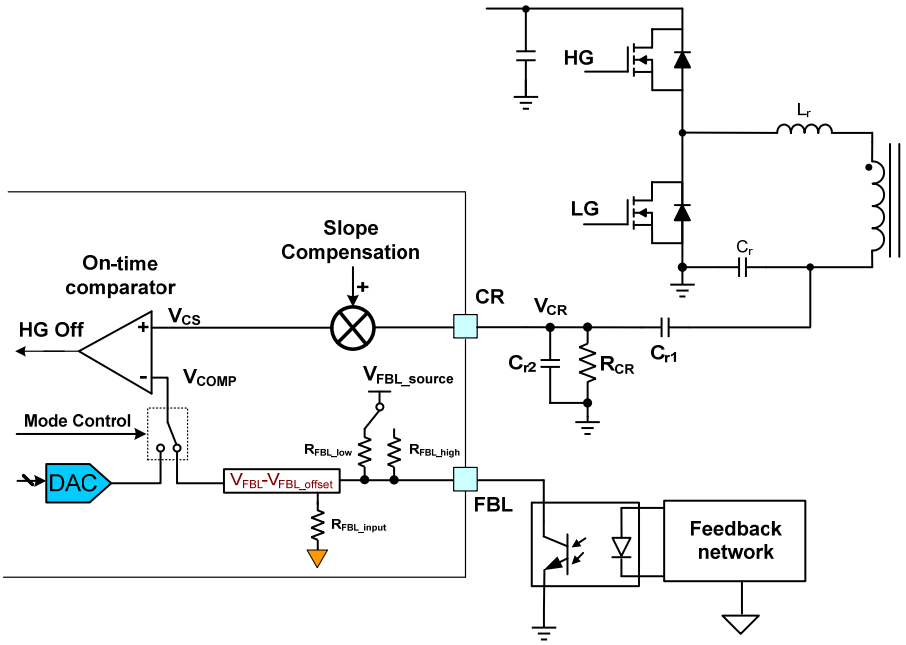


Figure 68: CR pin sensing circuit

The resonant current I_{Lr} is calculated by Equation (49):

$$I_{Lr}(t)=\sqrt{\left(\frac{\pi\cdot Io}{2\cdot N_T}\right)^2+\left(\frac{N_T\cdot Vo}{4\cdot Lm\cdot fr0}\right)^2}\cdot\sin(2\pi\cdot fr0\cdot t) \tag{49}$$

Where Io is the LLC output current, N_T is the turn ratio of LLC transformer, Vo is the LLC output voltage, Lm is the magnetizing inductance of LLC transformer, $fr0$ is the resonant frequency.

The voltage on resonant capacitor is calculated with Equation (50):

$$V_{Cr}(t)=\frac{1}{2}\cdot\frac{\int_0^{T0}I_{Lr}(t)dt}{C_r}\cdot\sin(2\pi\cdot fr0\cdot t)+\frac{V_{bus}}{2} \tag{50}$$

Where T0 is the switching period.

The resonant capacitor voltage difference ΔV_{Cr} is the V_{Cr} removed the DC bias, which is calculated with Equation (51):

$$\Delta V_{Cr}=\frac{\int_0^{T0}I_{Lr}(t)dt}{C_r} \tag{51}$$

The CR pin voltage is calculated with Equation (52):

$$V_{CR}=\frac{\frac{Xc(Cr2)\cdot R_{CR}}{Xc(Cr2)+R_{CR}}}{Xc(Cr1)+\frac{Xc(Cr2)\cdot R_{CR}}{Xc(Cr2)+R_{CR}}}\cdot\frac{\Delta V_{Cr}}{2} \tag{52}$$

Where Xc(C) is the impedance of a capacitor under resonant frequency, which is calculate with Equation (53):

$$Xc(C) = \frac{1}{2\pi \cdot fr0 \cdot C} \quad (53)$$

Under full load, V_{COMP} is V_{FBL}-V_{FBL_offset}, there is about 80kΩ input resistance of V_{FBL}-V_{FBL_offset} Amplifier, thus, the maximum V_{COMP_max} is $\frac{80k\Omega}{8k\Omega + 80k\Omega} \cdot 2.6V - 1V \approx 1.36V$ (the R_{FBL_low} is 8kΩ, the FBL source is 2.6V, the V_{FBL_offset} is 1V). Considering overload ability, the relationship of Vcomp_full and V_{CR} under full load is calculated with Equation (54):

$$V_{CR} = V_{COMP\_full} \approx \frac{V_{COMP\_max}}{Ratio_{overload}} \quad (54)$$

Where $Ratio_{overload}$ is $\frac{\text{Over Load Power}}{\text{Full Load Power}}$. The recommended C_{r1} is 110nF, and the recommended R_{CR} is 2kΩ. Therefore, the C_{r2} value can be calculated through the Equation (49) to Equation (54).

5.8.2 CSHB Sensing Circuit

The HR1211 can adopt two approaches for sensing current, i.e. capacitor divider based lossless current sensing and sense resistor current sensing. Generally, lossless current sensing is preferred in high-power applications (see Figure 69).

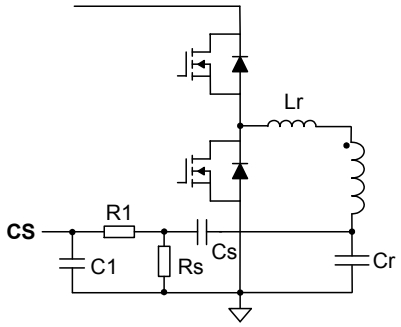


Figure 69: CSHB pin sensing circuit

To design the lossless current sensing network, the following inequalities should be satisfied:

$$Cs \le \frac{Cr}{100} \quad (55)$$

To prevent CSHB signal always less than the capacitive detection threshold V_{CSPR} (or V_{CSNR}) in light load, R_S should fulfill the condition below:

$$Rs > \frac{V_{CSPR}}{I_m} \cdot \left(1 + \frac{Cr}{Cs}\right) \quad (56)$$

Where I_m is the peak magnetizing current in the Equation (57):

$$I_m = \frac{V_{bus}}{8 \cdot Lm \cdot f_{max}} \quad (57)$$

Where f_{max} is the maximum switching frequency.

On the other hand, Rs shall be smaller than the equation below with a de-rating of 30%:

$$Rs \le \frac{0.7 \cdot V_{CS-OCP}}{I_{Crpk}} \cdot \left(1 + \frac{Cr}{Cs}\right) \quad (58)$$

Where I_{Crpk} is the peak current of the resonant tank at low input voltage and full load. I_{Crpk} can be expressed in Equation (59):

$$I_{Crpk} = \sqrt{\left(\frac{\pi \cdot Io}{2 \cdot N_T}\right)^2 + \left(\frac{N_T \cdot Vo}{4 \cdot Lm \cdot fr0}\right)^2} \quad (59)$$

R1 and C1 network is used to attenuate switching noise in CSHB pin. The time constant should not be larger than 100ns.

An alternative solution is to use a sensing resistor in series with the resonant tank (see Figure 70). This method is simpler with less external components, but may cause undesired power consumption on the sensing resistor.

Considering a de-rating of 30%, the sense resistor can be designed using inequality:

$$Rs \le \frac{0.7 \cdot V_{SCP\_LLC}}{I_{Crpk}}$$

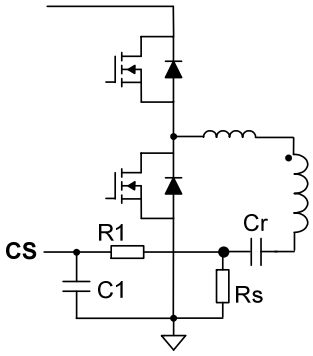


Figure 70: Current Sensing with a Sense Resistor

6. SYSTEM FLOW CHART

Figure 71 shows the system flow chart of the HR1211.

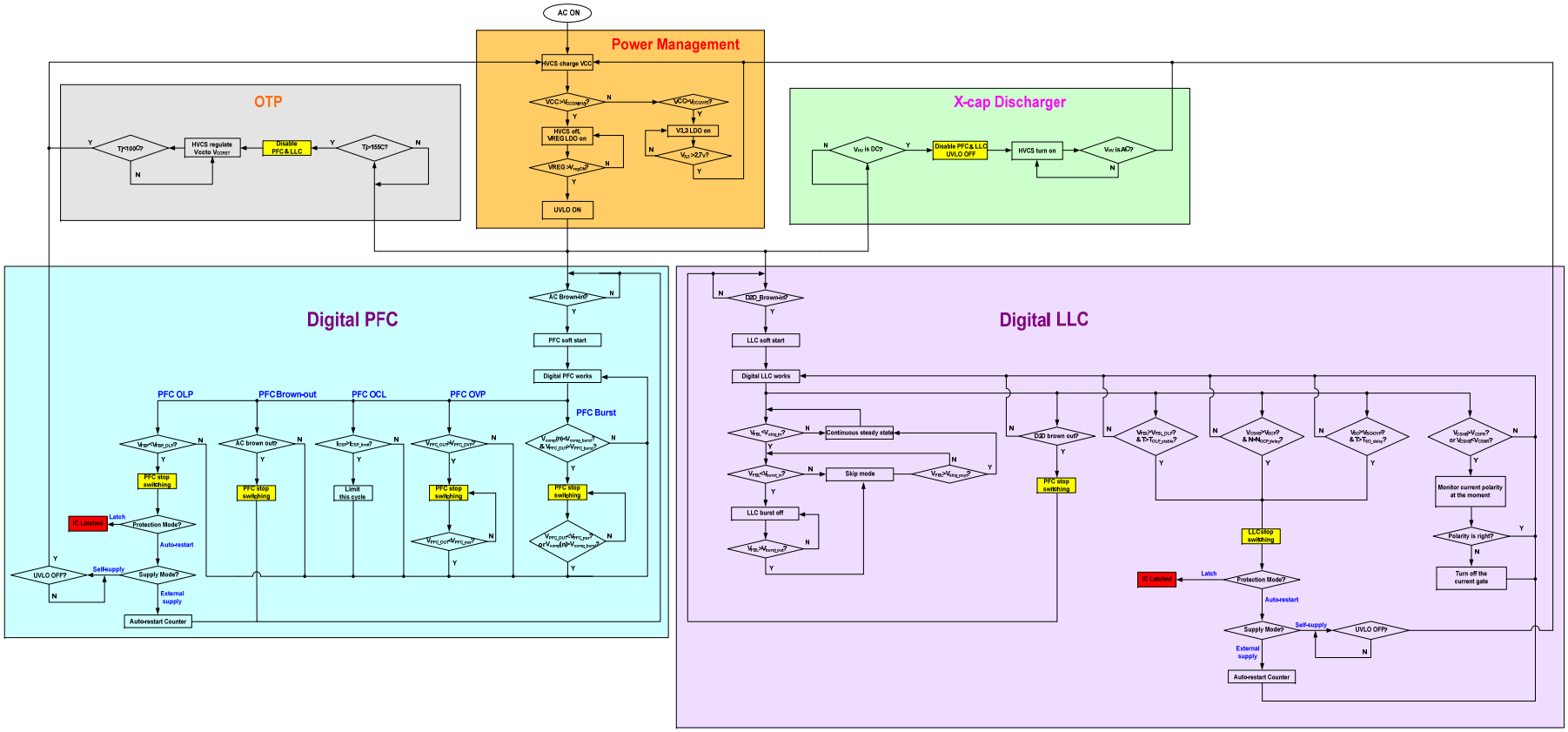


Figure 71: System Flow Chart

7. SUMMARY OF PROTECTION FUNCTIONS

Table 7: Overview of All Protection Functions of the HR1211

Pin	Symbol	Description	Affected	Action
VCC	V_{CC_UVP}	Under-voltage protection for VCC	System	Disable IC
VCC	V_{CC_SCP}	Short-circuit protection for VCC	System	Disable and limit I_{HV}
VREG	V_{Vreg_UVP}	Under-voltage protection for VREG	System	Disable and limit I_{ch}(Vdd)
	OTP	Over-temperature protection	System	Disable IC
ACIN	BI/BO	Line input under-voltage protection	PFC	Suspend PFC switching
CSP	OCL_PFC	Cycle-by-cycle current limit	PFC	Turn off PFC gate cycle-by-cycle
FBP	OVP_PFC	Over-voltage of PFC	PFC	Suspend PFC switching
FBP	OLP_PFC	Open-loop protection	System	Auto-restart / Latch
FBP	LLC brown-in/out	LLC stage under-voltage protection	HBC	Suspend LLC switching
CSHB	OCP_HBC	Over-current protection HBC	System	Auto-restart / Latch
CSHB	CMP	Capacitive mode protection	HBC	Turn off LLC gate cycle-by-cycle
SO		Multipurpose protection	System	Auto-restart / Latch

8. LAYOUT

This section describes the key considerations of routing and placing key components on the layout.

8.1 Power Stage

In Figure 72, Loop1~Loop4 are the high di/dt current loop, so the loop area should be as small as possible. To avoid cross-talk interference between the PFC and LLC, the trace of the power GND should be in a cascaded connection. For example, if the D point is directly connected to the B point without going through the C point first, crosstalk occurs between Loop2 and Loop3.

The three high dV/dt traces are shown in Figure 72. These traces are the noise source of common mode (CM) noise and radiated EMI, so the trace should be kept as short as possible.

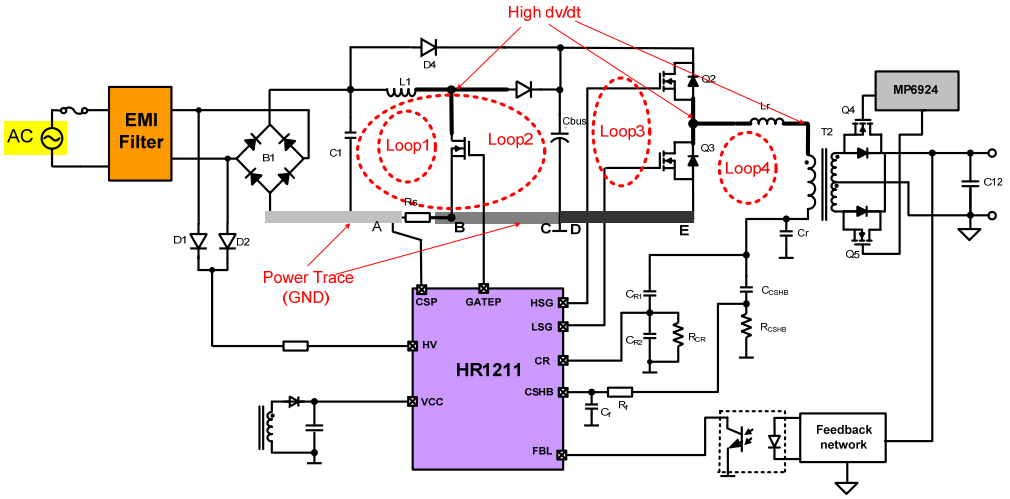


Figure 72: Consideration for Power Stage

8.2 Grounding

There are two different reference grounds in the HR1211: GNDD and PGND (see Figure 73). GNDD is the reference ground of various signals of the digital section, such as internal V3.3, ACIN, CSP, FBP, CR, CSHB, SO, UART. PGND is the reference ground of analog section, such as HV, VCC, VREG, GATEP and LSG.

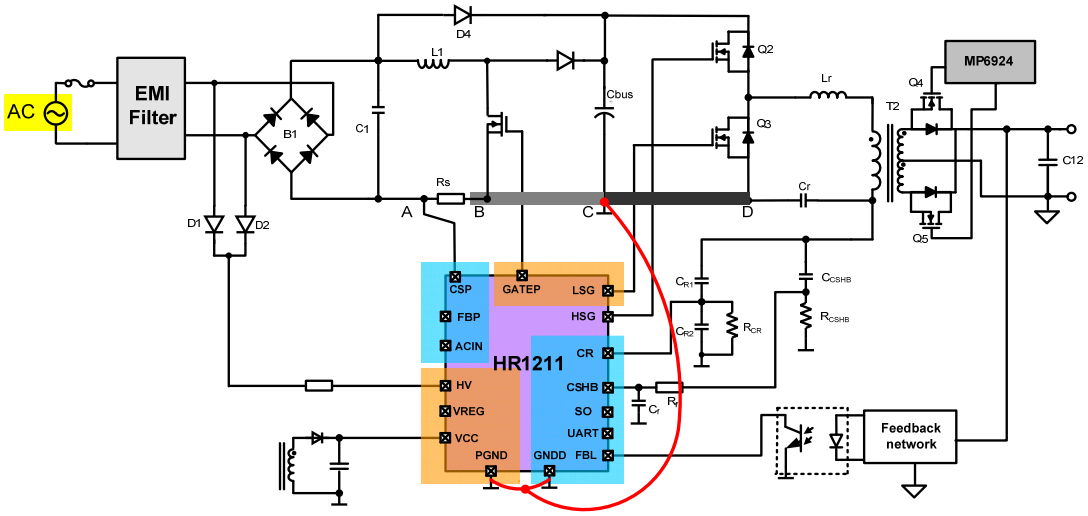


Figure 73: Reference GND

It is recommended to connect PGND and GNDD and make a large ground pour area, then connect to the negative side of the power stage with a single-point connection to avoid cross-coupling from the power ground to the digital ground (see Figure 73). The signal sensing filter capacitors' ground and VCC, VREG filter capacitors' ground should be connect to the ground pour area separately.

To prevent the PFC current distortion, the power ground trace (Point B to C in Figure 73) should be as short as possible.

Figure 74 shows an example of the GND connection in the single-layer board. PGND and GNDD are connected together and make the ground area as large as possible under IC, and then connected to the negative port of the bus capacitor directly.

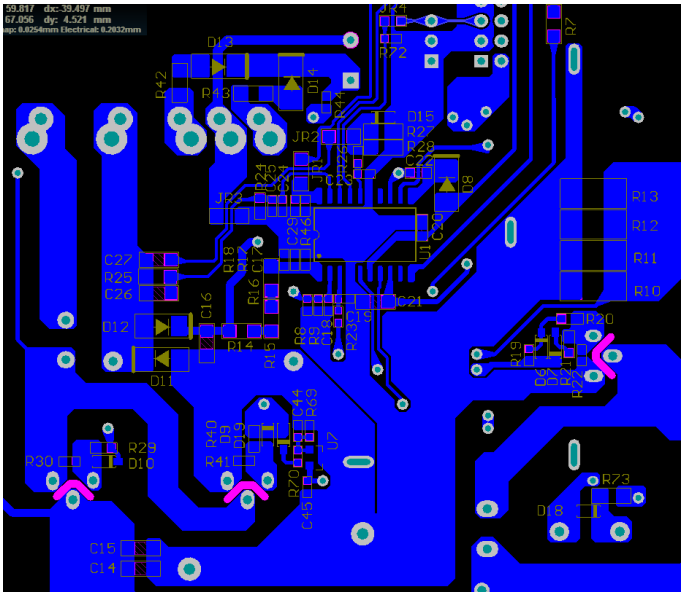


Figure 74: Layout Example

8.3 Key Signals

The key signals that might be disturbed by noise and deteriorate performance are CSP, CR, CSHB and FBL, described as below.

- **CSP:** The current of the PFC inductor becomes distorted if the CSP signal is disturbed by other noises, which may worsen THD, PF, and even the audible noise. To reduce noise coupling, the loop formed by PFC inductor current sense, CSP and GND should be as small as possible (see Figure 75).
- **ACIN:** The ACIN sensing circuit trace is usually away from the IC because it sensing the voltage before the rectifier bridge. It is recommended to place whole sensing circuit to near the IC (see Figure 75) to improve the anti-interference ability. The pull-down resistor and filter capacitor should be as near the IC as possible.
- **CR:** CR is the resonant capacitor voltage sense for the LLC stage. The signal is used for on time comparator input, which decides the HSG turn on time. The loop of CR sensing circuit should be as small as possible.
- **CSHB:** CSHB is the resonant current sense of LLC stage, and is used for capacitive mode protection and short circuit protection. The R-C filter should be placed close to CSHB, and the loop should be small.
- **FBL:** FBL is the feedback signal of the LLC from the collector of the optocoupler. The trace connecting to the collector should be as short as possible and as far away from the high dV/dt

trace as possible (e.g.: the trace in the middle point of the half bridge). If this signal is disturbed by other noises, duty unbalance of the LLC occurs and may cause the LLC to work abnormally. It is highly recommended that the trace be placed in parallel with the trace of the return signal and to make the loop area as small as possible.

- **UART:** UATR provide a half-duplex communication IO interface. UART is recommended to parallel with a 100pF capacitor to GND in case suffering the disturbance.
- **HV:** HV pin is use to detected input voltage for the X-cap discharge function. A resistor (about 2KΩ to 10KΩ) is recommended to prevent the surge shock. The trace between the resistor and HV pin should be away from the high dV/dt trace and component.

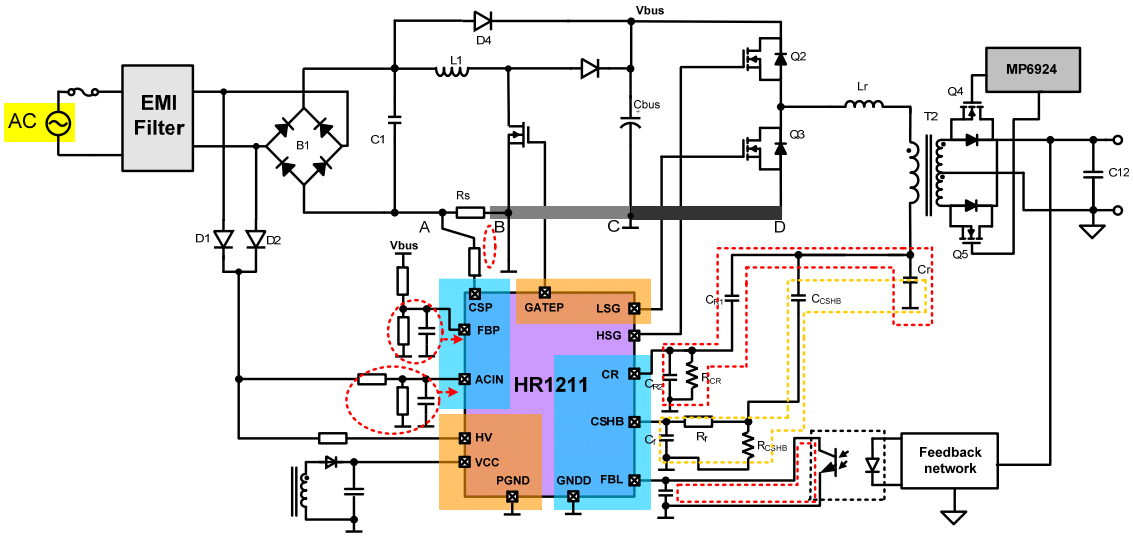


Figure 75: Key Detection Signals

8.4 Key Component Placement

The key components should be given careful consideration during layout. Refer to Figure 76 and follow the guidelines below.

1. Place the noise decoupling cap of ACIN, FBP, CSHB and FBL as close to the IC as possible.
2. Place C_{R2} as close to the IC as possible.
3. Place the HR1211 away from the high dV/dt components of the LLC stage (e.g.: Lr and T2).
4. Connect VD1 (Light-Load Mode detection pin) of MPS synchronous rectification controller to the Loop corresponding LSG on, in case SR controller enters light-load mode when HR1211 works in skip mode.

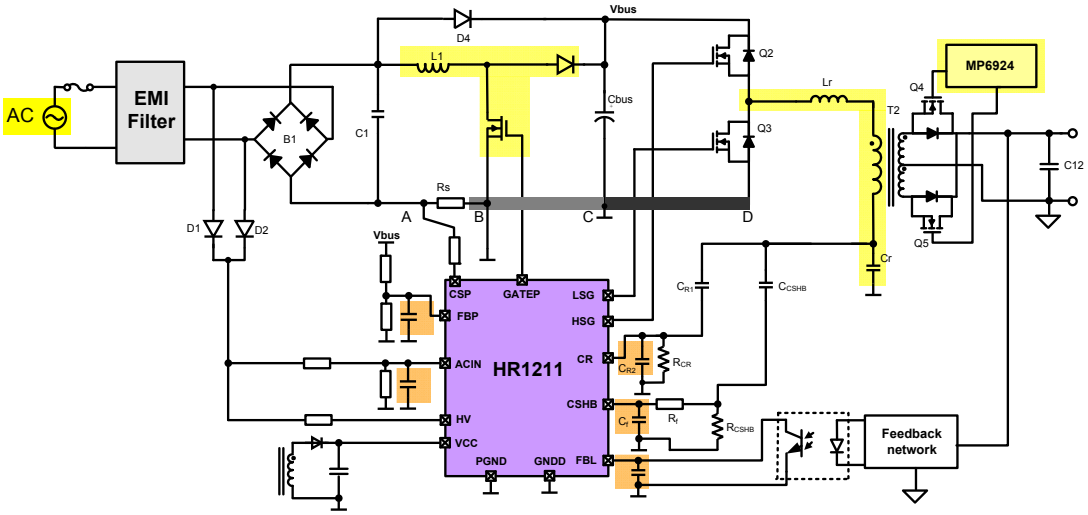


Figure 76: Key Component Placement

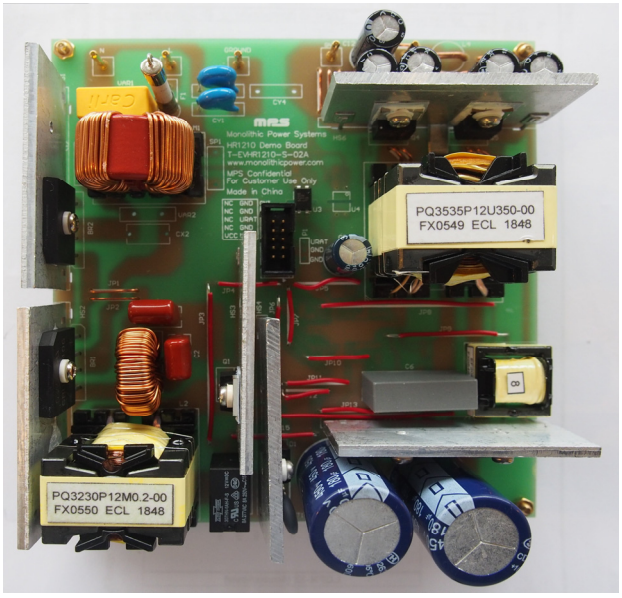
9. DESIGN EXAMPLE

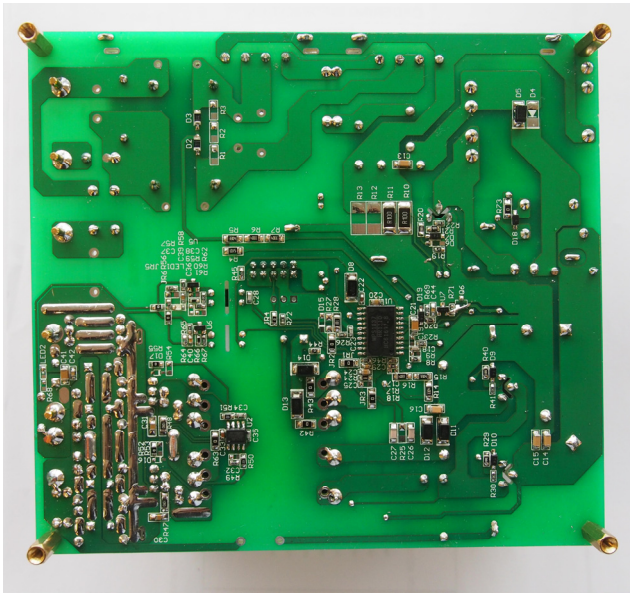
The EVB is designed for verification and evaluation of the performance of the HR1211. For details of the EVB, please refer to the EVB datasheet.

9.1 Design Specification

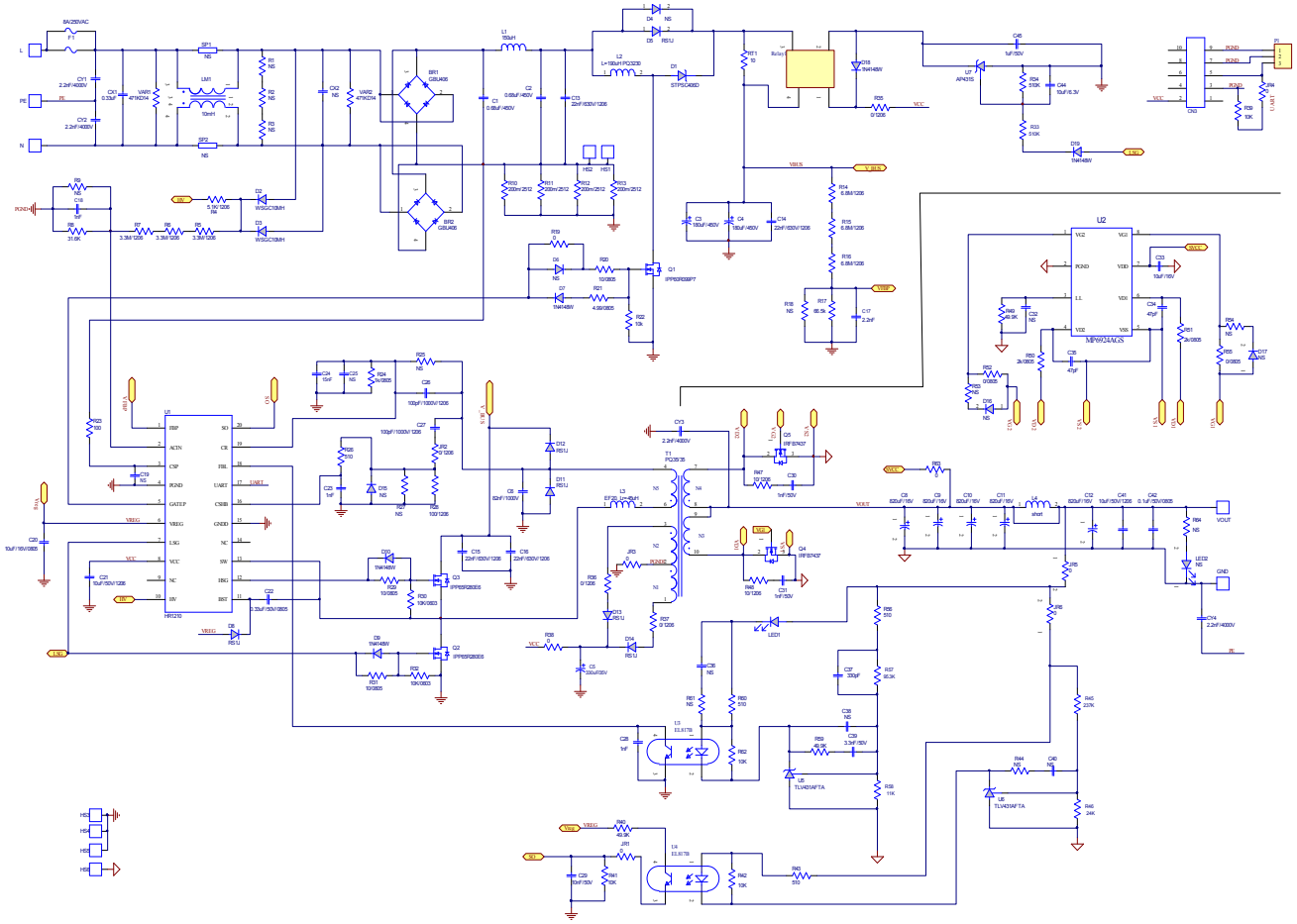
Parameter	Symbol	Condition	Min	Typ	Max	Units
Input supply voltage	V_{AC}	2-wire or 3-wire, full load range: $90V_{AC}$ - $264V_{AC}$	90		264	V
AC line frequency	F_{LINE}		47	50/60	63	Hz
Output voltage	V_O			12		V
Output current	I_O			33.3		A
Output voltage ripple	V_{O_ripple}	V_{AC} = 230V, full load		100		mV
Continuous output power	P_O			400		W
Efficiency	η		80+ platinum			%
Start-up time	t_{ST}				2	S
Power Factor		V_{AC} = 90V to 264V, full load	0.9			
THD		V_{AC} = 90V to 264V, full load			10%	
Conducted EMI			Meets EN55022 Class B			
Harmonics			Meets IEC61000-3-2 Class C			
OCP			Auto-restart			
OVP			Latch			
Operation temperature	T_{AMB}	Free convection, sea level	-40		70	°C

9.2 EVB



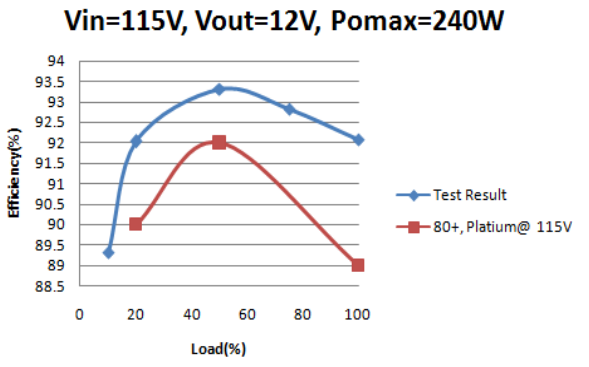


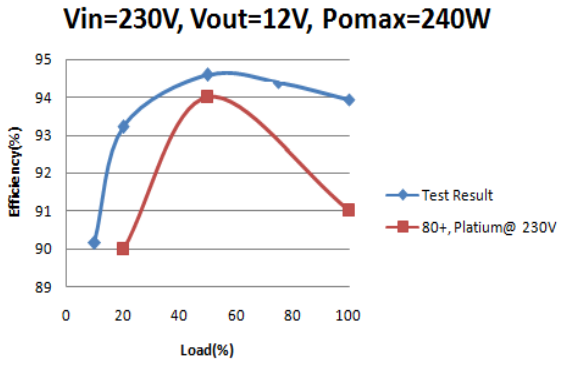
9.3 Schematic



9.4 Performance

- **Efficiency**

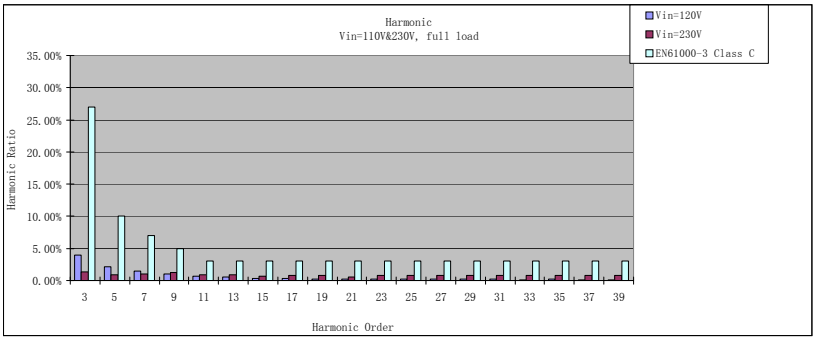




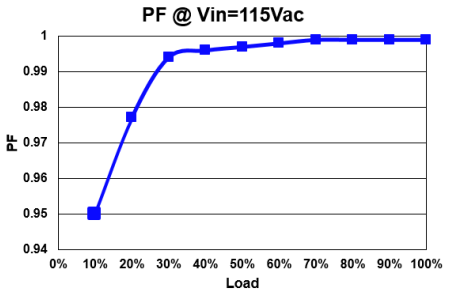
- **No Load Consumption**

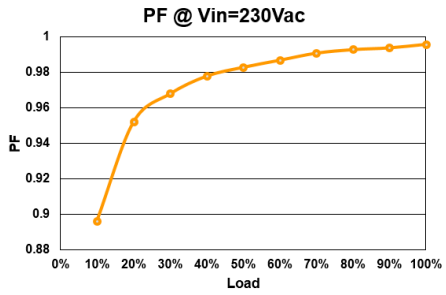
Vin (Vac)	90	115	230	264
Pin (mW)	82.7	84.9	93.6	96.6

- **Harmonics**

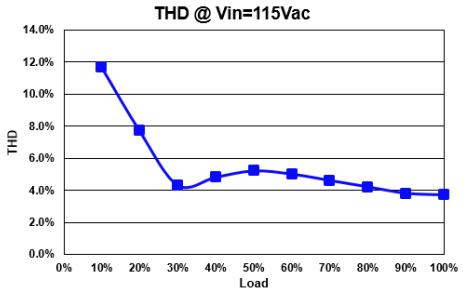


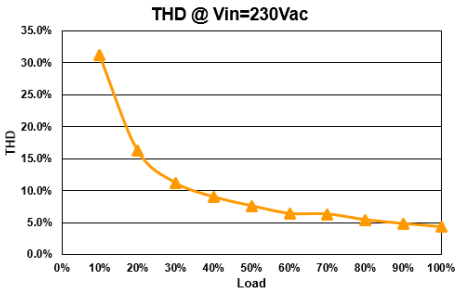
- **PF**





- **THD**





- **EMI Test Result**