Challenges and early review of your design!

Why we fail in EMC and how to avoid it.

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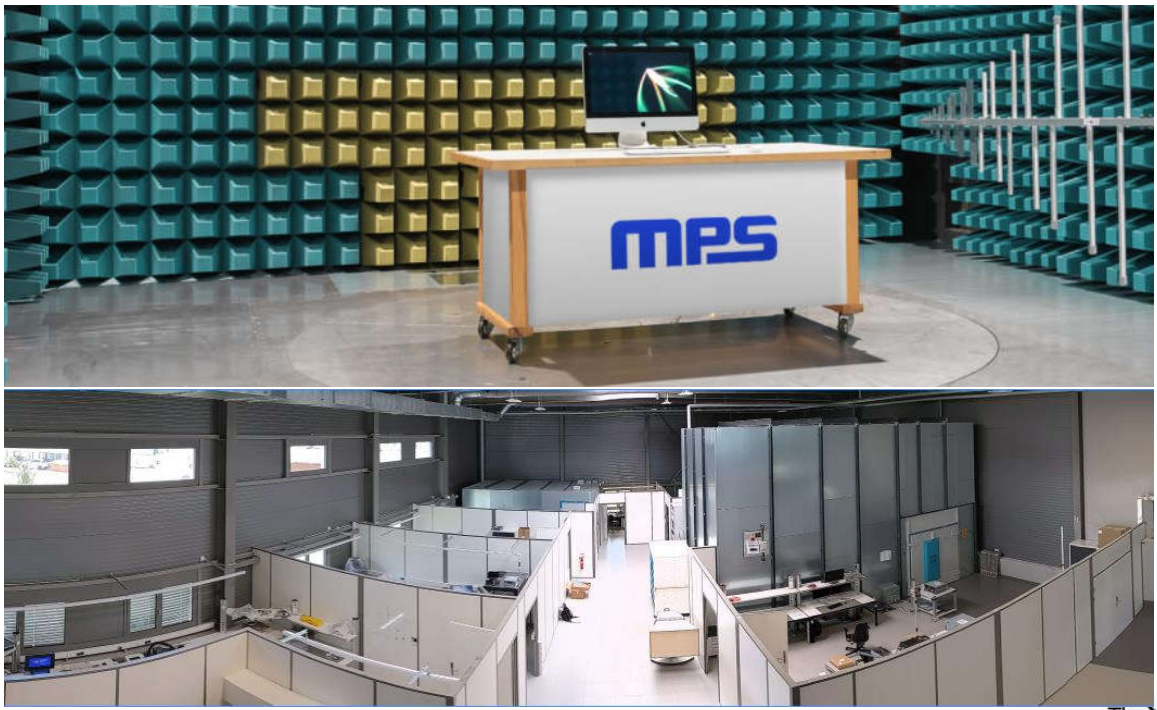
Organized by:

ROHDE&SCHWARZ
Make ideas real

Nov 2021

EMI/EMC/SI Design and Troubleshooting

Congrats: what a great laboratory!



Two exciting days: ... for EMI/EMC!

DAY 1: 9th November

9:30 to 12:00 (CET) – Roots of EMI (Part 1)

> Challenges and Early Review of Your Design! (Presented by Arturo Mediano, University of Zaragoza - 45min)
> EMC Testing from First-Level Debugging to the Compliance Stage (Presented by Christian Reimer, R&S - 45min)
> Practical and Early Testing Showcases (Presented by Jan Spindler, MPS - 45min)

Register Now

13:00 to 16:30 (CET) – Roots of EMI (Part 2)

> EMI Troubleshooting and Debugging (Presented by Arturo Mediano, University of Zaragoza - 1h)
> DC/DC Conversion Workshop – DUT Troubleshooting (Presented by Jens Hedrich, MPS - 1h)
> Pre-Compliance Set-Up (Presented by Alexander Küllmer, R&S - 1h)

Register Now

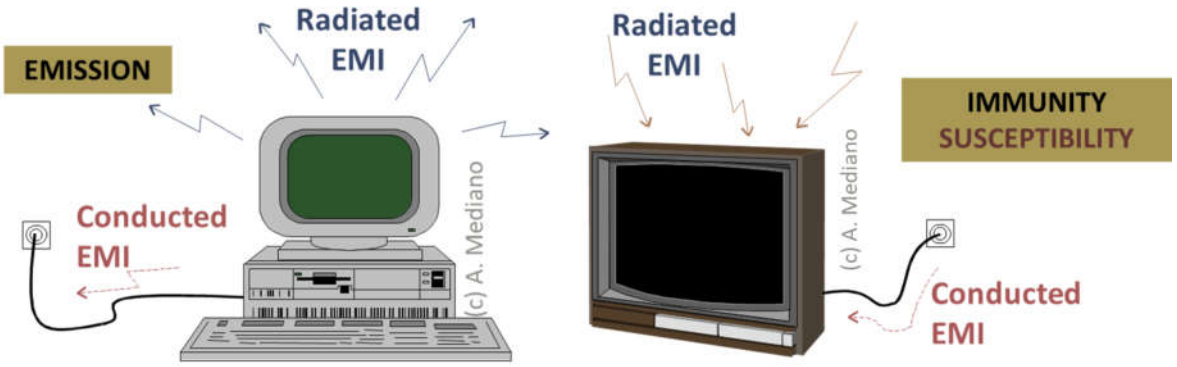
DAY 2: 10th November

8:30 to 12:00 (CET) – Power Applications

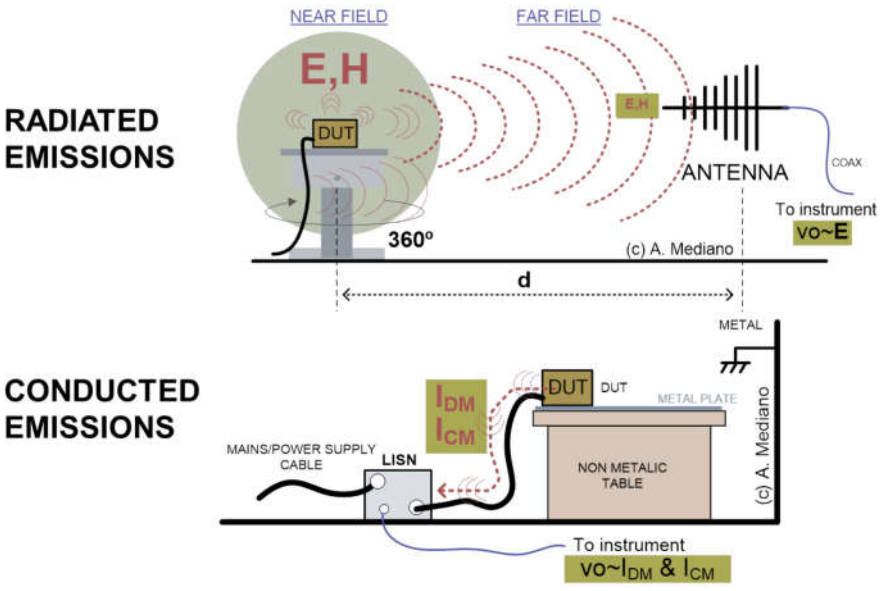
> Filter Design Hints and Tricks (Presented by Arturo Mediano, University of Zaragoza - 45min)
> Stability in Converters: Control Loop & Load Step Design (Presented by Christian Kueck, MPS - 45min)
> Power Integrity Can Cause EMI Challenges (Presented by Arturo Mediano, University of Zaragoza - 45min)
> Mythbusting EMC Techniques in Power Converter Design (Presented by Francesc Estragues, MPS - 45min)

EMI/EMC: classification

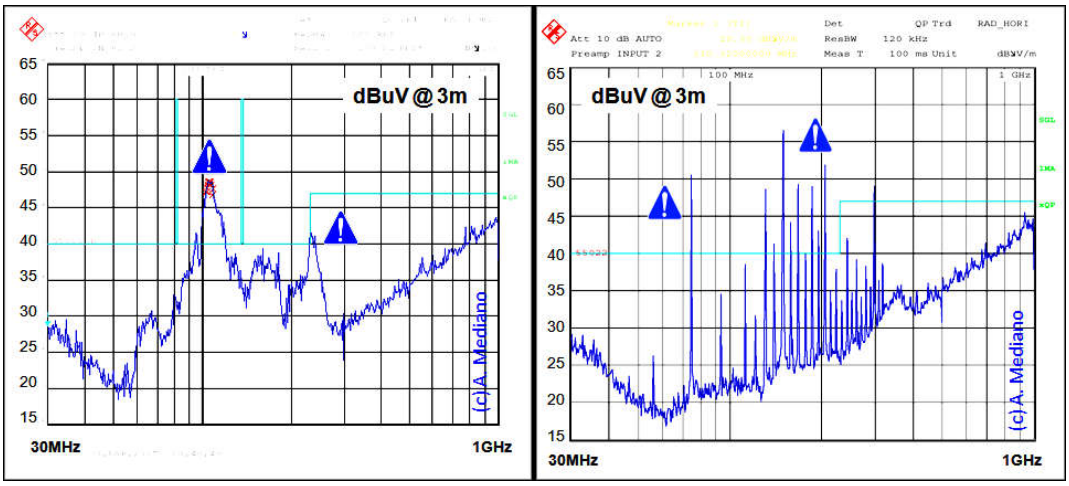
Radiated and conducted **emissions/immunity**



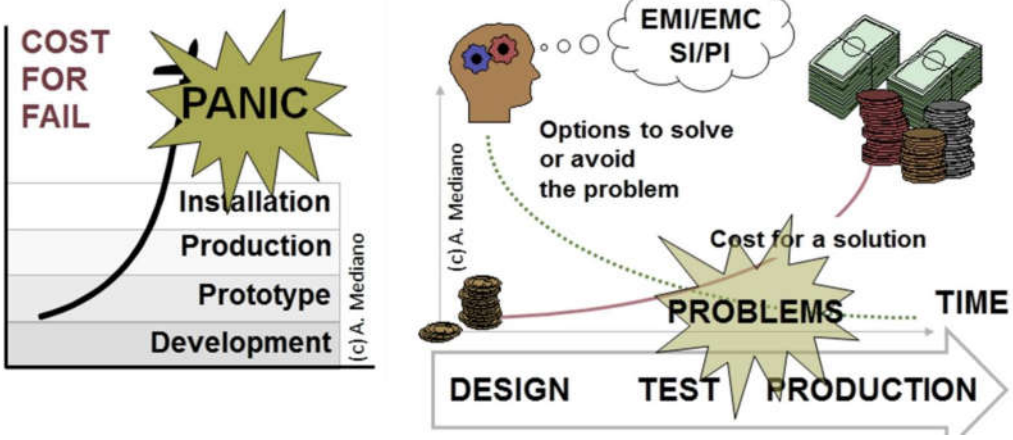
EMI/EMC: tests



Introduction: example failures



It is time for failures: too late?



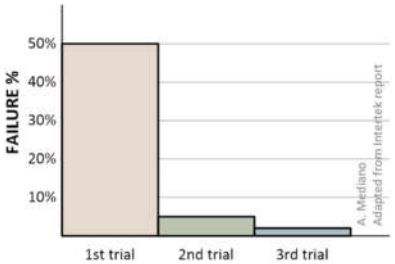
EMI/EMC: why it is a headache?.....

- **Delays to market**
  - weeks for "easy" problems
  - months for difficult problems
- **Unexpected costs(thousand** $/€)
  - redesign - retesting - consultants
- **Need for tests** (external and internal) = time + cost
- **Image degradation** for customer/market
- **Size**
- **Weight**
- **Failures in the field (immunity)**
  - Returned products because ESD, EFT, transients,
- **Stress**

EMI/EMC/SI Design and Troubleshooting

EMC failures: why we fail?. Some causes ....

- **No time**
  - We will "do the EMC" later!
- **Assume the product will pass EMC first time**
  - Companies leave EMC pass-fail at lab up to chance
  - Global EMC first time pass rate ≈ 50% ------->
- Applying **incorrect EMC regulations**
- Use of **non-compliant modules or components**
- **No EMC knowledge**
  - Difficult subject
  - No experience/knowledge in high frequency
  - Special measurement techniques are required
  - Hidden schematic and unexpected-parasitic effects = Magic!
- **Late response**
  - Start EMC analysis when customer is notified the product is finished
  - Pass the final product to the EMC engineer to "do the EMC"
  - In the meantime change the design without notification to the EMC engineer.
  - If the product fails, put the EMC engineer to work in the weekends!
  - If no success, do not worry, can the problem be solved by software?



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EMC failures: early review!!!!

A TYPICAL "FUNCTIONAL" REVIEW PROCESS IN ELECTRONICS:

- ❑ voltage and current checks
- ❑ firmware functionality
- ❑ efficiency and stress
- ❑ connector pins check
- ❑ mechanical conflicts
- ❑ symbol to footprint coherence
- ❑ costs reviews
- ❑ etc .....

WHY NOT TO DO SOMETHING SIMILAR FOR EMC?

Create your own **design check list**!
Not necessarily companies with EMC experts are doing EMI/EMC review

This presentation only includes general ideas

EMI/EMC/SI Design and Troubleshooting

EMI/EMC review: general ideas

- **The EMC design review is mandatory to detect bad design practices.**
- **Both emissions and immunity must be considered.**
- **Add experience to your design review process**
- **Look for the limits, levels, and tests** you need to pass in emissions and immunity.
  - where you want to market your product
  - environments: industrial, residential , etc.
  - special requirements from customers

Example choosing switching frequency

- **Consider:**
  - technologies/packages/ICs review
  - schematic review
  - PCB review
  - mecahnical design review
  - cables review
  - firmware ideas
  - test prototypes

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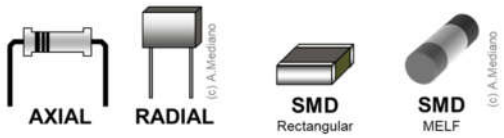
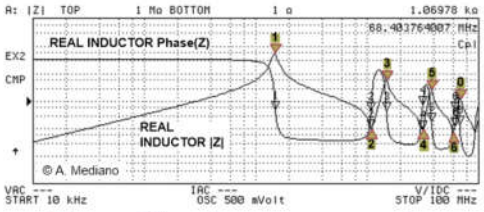
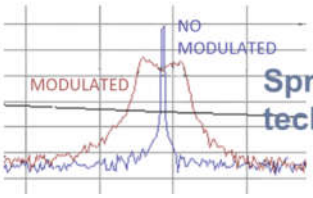
EMI/EMC review: technologies/packages/ICs



SMD versus through-hole

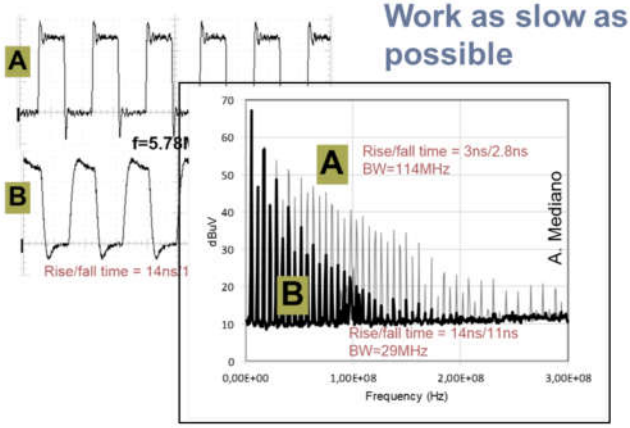


Parasitics in components



Spread spectrum techniques

Work as slow as possible



Rise and fall times
Evaluate low cost "equivalents"
Too fast diodes?
Low EMI versions
Etc, etc.....

EMI/EMC/SI Design and Troubleshooting

EMI/EMC review: schematic review

Added test points?

GND symbols?

Transient protection in I/O pins?
Decoupling and PDN design (PI)
- some IC or circuit without good decoupling?
- how many caps? what technologies?

Instructions for layout designers?
- especially critical if PCB design is outsourced!
- clean and documented schematics is critical
- shielded areas
- notes/explanations

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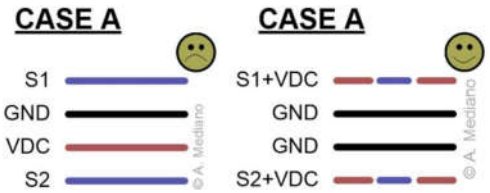
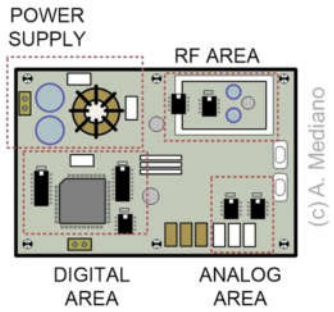
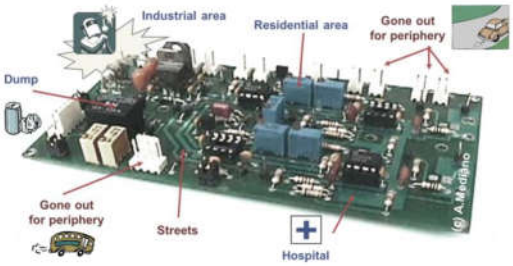
EMI/EMC review: PCB

PCB stack-up and number of layers
be careful with 1-2 layers! (typical for low cost products)
really cost 2 layers + EMI filters/components < cost 4 layers?



Number of boards in your system. Interconnection.
PCB zoning/partitioning/placement



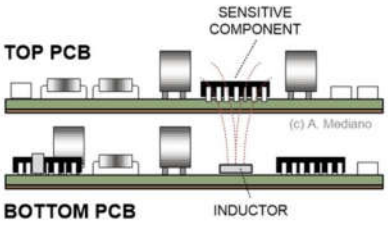


EMI/EMC/SI Design and Troubleshooting

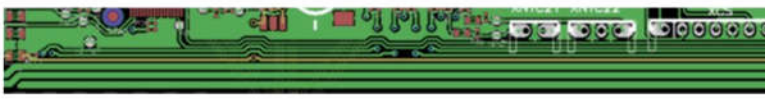
EMI/EMC review: PCB

DRC tool!

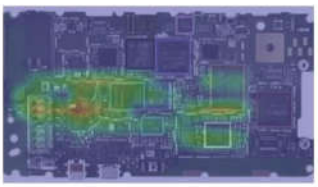
Component location
DC/DC converters
inductors (H field)

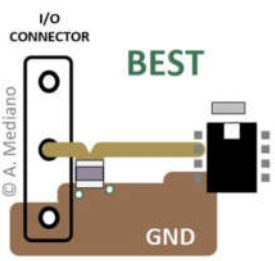


Layout
Critical signals in edge?
Avoid long traces. Avoid loops.
Distances between critical traces: safety & crosstalk
Critical signals layout: RF, high speed, low level analog, resets/Enable/IRQ, I/O signals, etc.
High speed layout and terminations (SI)



Desensing risks?





Transient protectors selection and placement

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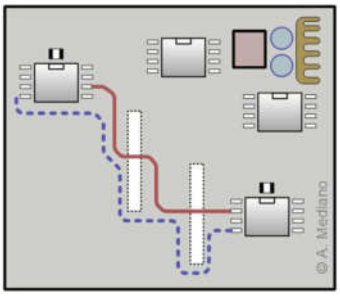
EMI/EMC review: PCB

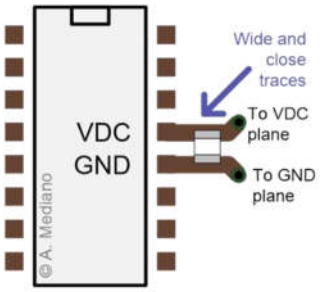
DRC tool!

Ground system (planes)
Slots in ground planes



Critical areas far from I/O connectors.

Decoupling and PDN design (PI)
how are the decoupling caps placed and routed?
check by simulation if possible



Shields in PCB?

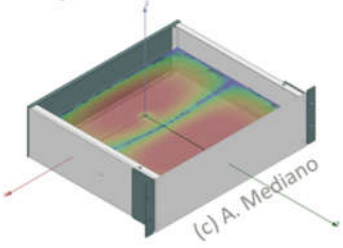
- agressive areas and sensitive areas
- connection to GND without slots
- filtering I/O traces (i.e. X2Y caps)

Guards

EMI/EMC/SI Design and Troubleshooting

EMI/EMC review: mechanical design (1)

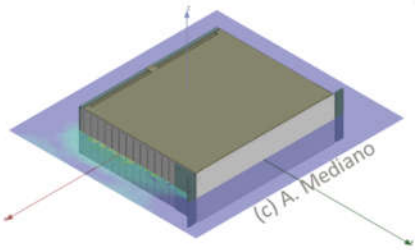
Enclosure resonant frequencies



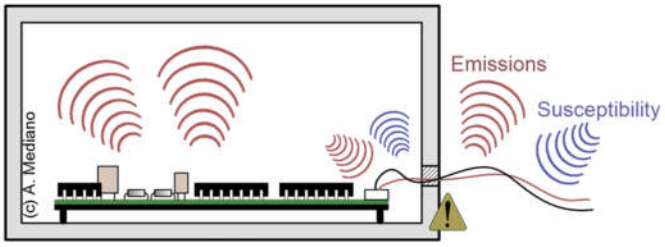
Test shielding in parallel with electronic design

Seams/slots/apertures

- non metalic paints
- holes/ventilation far from agressive/sensitive areas
- use of gaskets?



I/O cables filtered



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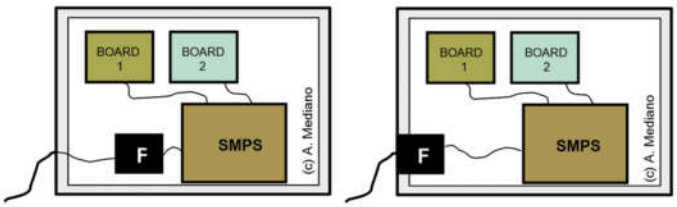
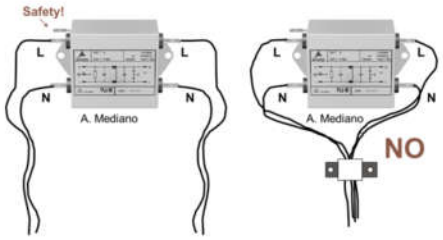
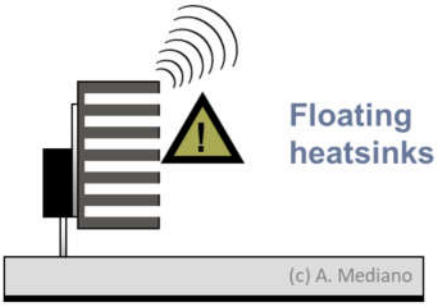
EMI/EMC review: mechanical design (2)

Filter location



Filter I/O feedback

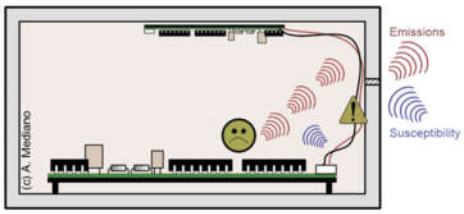




Floating heatsinks

Cables close to slots?

Cables close to slots & seams

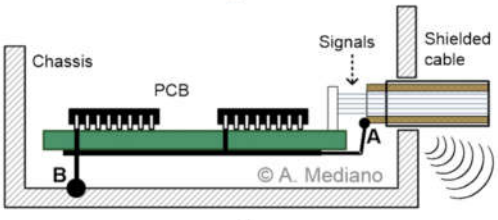


EMI/EMC review: cables

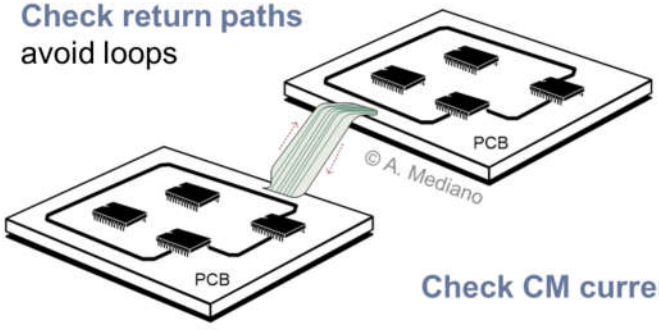
Main antennas for 30-400MHz range
Do you need uniform TX lines?

Ideal number of cables = 0.
Minimize cable number
Minimize length

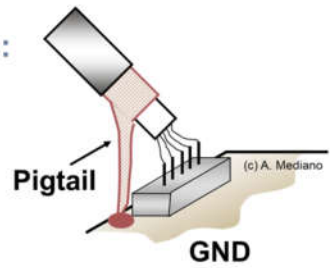
Shield connections to enclosure, not to gnd



Check return paths
avoid loops



Avoid pigtails:



Check CM currents <µA

EMI/EMC review: firmware

VERY IMPORTANT FOR IMMUNITY

- watchdog timers
- checkpoints, checksums, error detection/correction, ...
- average of measured values.
- confirm read/write in digital ports periodically
- etc.

VERY IMPORTANT FOR EMISSIONS

- Stop non used signals (i.e. accessories not connected)
- Stand-by in critical areas while not in use (i.e. clocks)
- Spread-spectrum techniques in digital and power electronics

EMI/EMC/SI Design and Troubleshooting

EMI/EMC review: test prototypes

- **Pre-compliance instrumentation**

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THANK YOU!

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